# Lyapunov Redesign of Classical Digital Phase-Lock Loops

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## Abstract

**The author has previously established that Lyapunov redesign is effective in designing an analog phase-locked loop for which the nonlinear model (in the signal phase space) is guaranteed to be stable [1]. This paper extends that concept to what are commonly called classical digital phase-locked loops [2]. These loops, which are very common in high speed digital communications systems, use digital phase detectors but analog filters and VCOs.**

## 1 Introduction

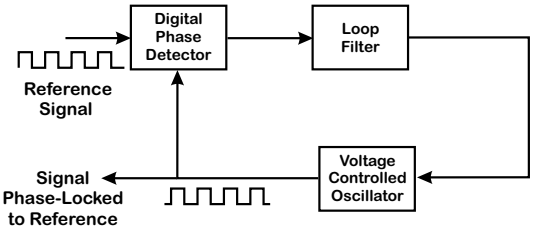


**Figure 1: A classical digital phase locked loop.**

There have been some more recent results in nonlinear analysis of analog PLLs [1, 3, 4, 5]. The task of this paper is to apply the technique of Lyapunov Redesign [6] to a class of digital PLLs. This paper will describe the class of digital PLLs known as classical digital phase-locked loops (CDPLL) [2], describe a set of digital phase detectors used in these loops, and show how a parallel development to the author's earlier work [1] can be applied to these loops.

Typically, stability analysis deals with noise free models. This will be the case here. While practical analysis and simulation of a real system must include some noise

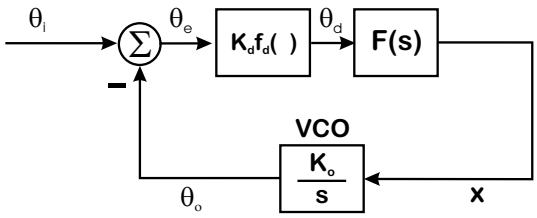


**Figure 2: Conceptual block diagram of PLL with digital phase detector. This is a transition stage in the analysis of the classical digital PLL. This model represents the effect of the digital phase detector once the high frequency component has been attenuated.**

model, a prerequisite for such analysis is either the knowledge or the assumption that the loop is stable. This paper will attempt to provide the former. Furthermore, stability analysis deals with the homogeneous (no input) differential equation of the system. This will be useful here, as it is often convenient to perform block diagram manipulations to give a set of states for which it is easy to extract stability results. Finally, stability is an asymptotic property. Knowing that a system is stable or that it tracks a step input does not in itself yield performance results. The purpose of this paper is to provide a design method for classical digital PLLs that will guarantee stability and tracking.

The structure of this paper is as follows. Section 2 will review the model of a classical digital PLL. Section 3 will describe a handful of digital phase detectors used in CDPLLs. Section 4 will introduce the necessary definitions and theorems for doing analysis. The actual analysis as applied to phase-lock loops will be done in Section 5.

## 2 Classical Digital PLL Basics

Generally speaking, there are a variety of reasons to use digital circuitry to implement PLLs rather than the classical methods. In this case analog voltage levels are often replaced by digital logic levels. For example, clock signals to drive digital circuitry, computers, and digital communications systems all run better with Walsh functions (rectangular waves) rather than sinusoids. In fact, several digital phase detectors are useful for detecting the phase of the underlying clock signal in digital data. This enables clock/data recovery (CDR) in digital communications and storage systems. Furthermore, these digital circuits are easier to integrate and verify than their analog counterparts. Finally, as the speed of the logic outstrips the speed requirements of the applications, such implementations become far more reliable than the classical methods.

While the development for the analysis of digital PLLs is more graphical and heuristic than that for analog PLLs [7, 8], similar results follow. Those are:

1. The high frequency portion of the phase detector response is attenuated by any high frequency low pass filter in the loop [7] and by the low pass nature of the PLL itself.

2. The VCO frequency, $\omega_o$, is close enough to the underlying clock frequency of the reference signal, $\omega_i$, that their difference can be incorporated into $\theta_e$. This means that the VCO can be modeled as an integrator.

Making these assumptions leads to the PLL model shown in Figure 2.

The analysis of this paper is applied entirely to the baseband model of the classical digital PLL (CDPLL) as defined by Best [2] and shown in Figure 2. The name is somewhat of a misnomer from the controls perspective. It is not a digital, sampled data system as the term digital would imply to control theorists. Instead, it is an analog PLL implemented with a digital phase detector, such as one of those in Section 3. In this case, the output of the digital phase detector is seen as a continuous time voltage and this voltage is fed to an analog loop filter. PLL authors point out that this type of PLL has all the disadvantages of the classical PLL due to its analog components. Still, this loop has advantages in that it can be implemented at very high frequencies (multiple Gigahertz) with fairly reliable logic. Furthermore, these loops can be analyzed using continuous time linear feedback theory. It is for this reason that some authors do not treat these loops as digital at all [8].

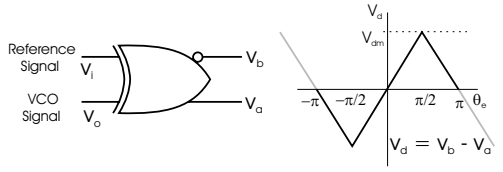


**Figure 3: Phase detection using an XOR gate. Note that this accomplishes the same thing as an over driven mixer, but with digital circuitry.**

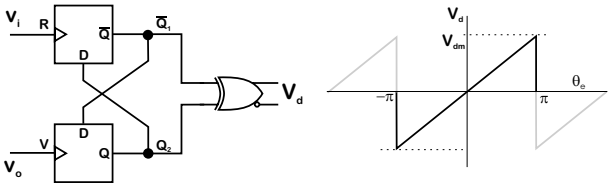


**Figure 4: Two state phase detection using gates. The two logic combinations result in the same PD characteristic.**

## 3 Digital Phase Detectors

This section will present a handful of digital phase detectors used in classical digital PLLs along with their baseband responses. A discussion of how these detector characteristics are determined can be found in several texts [2, 7, 8]. While these phase detectors have worse noise performance than the classic mixing detectors, they often have better pull in range and are much more manufacturable, especially for high speed applications. Furthermore, most of these phase detectors have advantage that their low frequency response is actually linear over some range rather than sinusoidal. The exception to this group is the Alexander or Bang-Bang phase detector [9], which as its name implies produces a response similar to that of a relay.

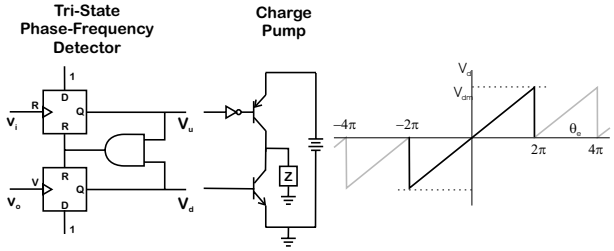


**Figure 5: The combination of a tri-state phase-frequency detector and a charge pump. Note that the loop filter is often implemented in the Z block of the charge pump.**

One of the simplest digital phase detectors is an Exclusive-OR (XOR) gate shown in Figure 3. One advan-

tage of such a phase detector is that the loop gain is now independent of input signal amplitude. The disadvantage is that the linearity of the baseband response is affected by the relative duty cycles of the input and VCO signals [8]. The baseband (low frequency) component of the signal behaves with the triangular phase response shown in the right of Figure 3 (for a 50% duty cycle of the input signal).

To eliminate the duty cycle dependence of the XOR phase detector, detectors using flip flops can be used. An example of this [8] is shown in Figure 4. The phase detector is only sensitive to the rising edges of the input signals, rather than their duty cycles. Furthermore, the linear region of the phase detector is expanded to $\pm\pi$ from $\pm\pi/2$. However, the phase detector is no longer memoryless, so noise spikes that are large enough to trigger a change of state have a larger effect than they do with the XOR phase detector. The resulting baseband component of the phase detector output now has a sawtooth, rather than triangle wave response, and so this detector is often called a sawtooth detector. A tri-state phase-frequency detector (PFD) with a charge pump shown in Figure 5 extends this idea and the linear region to $\pm 2\pi$ [8].

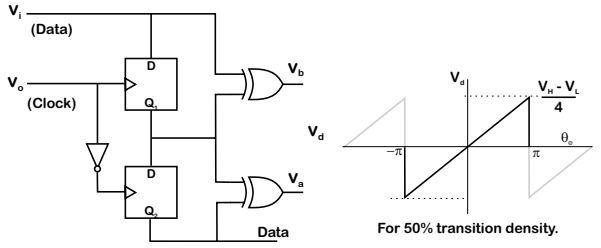


**Figure 6: The Hogge phase detector. Used primarily in clock data recovery applications (CDR), the Hogge detector has a linear characteristic. $\bar{V}_b$ is modulated by the signal phase while $\bar{V}_a$ is not. The difference gives a phase error for the data signal.**

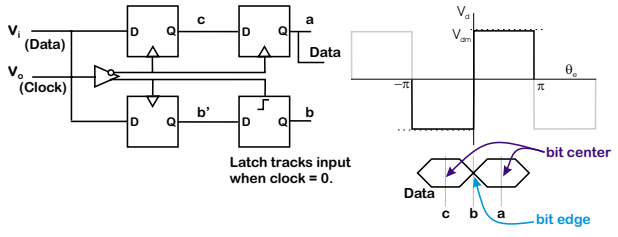


**Figure 7: The Alexander (bang-bang) phase detector. The original version made of component flip flops. The version shown here is a circuit well suited to integration which substitutes a latch for the last flip flop, thereby saving one latch. On the right is the phase detector characteristic.**

Clock recovery from a data stream, known as clock/data recovery (CDR), requires a special type of phase detector. One of the most popular is the so-called Hogge [10] detector, show in Figure 6. The Bang-Bang phase detector [9] shown in Figure 7 is unique among the detectors presented here in that its baseband behavior is never linear. Instead, the detector acts as a relay over the region from $-\pi$ to $\pi$.

# 4 Lyapunov Stability

The second method of Lyapunov[11] is commonly used in stability analysis of nonlinear differential equations because it does not require the solution to the differential equation. The second method of Lyapunov is based on the generalized energy in the system. If an energy like function of the system state (*i.e.,* a positive definite function of the state which is nonvanishing as long as the state is nonzero) is found which is constantly decreasing, then the system is asymptotically stable. A general form of a vector differential equation is:

$$\dot{x} = f(x,t) \quad \text{where} \quad x, \dot{x} \in R^n. \tag{1}$$

An equilibrium state is any state such that

$$f(x_e, t) = 0. \tag{2}$$

Usually, a transformation is made so that the origin of state space is an equilibrium state *i.e.,*

$$f(0,t) = 0. \tag{3}$$

**Theorem 1 (LaSalle's Theorem)** *[11] For the system defined by Equation 1, suppose there exists a positive definite scalar function of $x$, $V(x)$, such that $\dot{V}(x)$ is negative semi-definite i.e.,*

$$\begin{array}{lllllll} V(x) & > & 0, & & \dot{V}(x) & \leq & 0 \qquad \forall x \neq 0 \\ V(x) & = & 0, & & \dot{V}(x) & = & 0 \qquad x = 0 \\ V(x) & \rightarrow & \infty & as & \|x\| & \rightarrow & \infty. \end{array} \tag{4}$$

*Suppose also that the only solution of $\dot{x} = f(x,t)$, $\dot{V}(x) = 0$ is $x(t) = 0$ for all $t \geq 0$. Then $\dot{x} = f(x,t)$ is globally asymptotically stable.*

This theorem will prove to be quite useful in the next section. In general $V$ is known as a *Lyapunov function* if it satisfies either LaSalle's Theorem or Lyapunov's Main Stability Theorem [11]. It turns out in practice that Theorem 1 is often easier to satisfy. Another definition that is necessary is that of a sector nonlinearity.

**Definition 1 (Sector Nonlinearity)** *The function $\phi(\cdot,\cdot)$ is said to belong to sector $[\alpha, \beta]$ if*

$$\alpha y^2 \leq y\phi(t,y) \leq \beta y^2 \quad \forall y \in R, \ \forall t \geq 0.$$

In other words, a sector nonlinearity would belong to sector $[\alpha, \beta]$ if it fell in the shaded region of Figure 8.

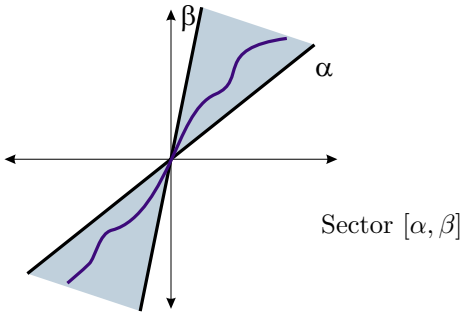


**Figure 8: Sector nonlinearity:** $\phi \in [\alpha, \beta]$

Lyapunov redesign starts with a candidate Lyapunov function. The function is parameterized by the design parameters of the system in question. These parameters are then chosen so that the candidate Lyapunov function meets the requirements of either Lyapunov's Theorem or LaSalle's Theorem. In this paper, that function will have the form

$$V = \int_0^z f(\sigma)d\sigma + x^T P x \tag{5}$$

which was introduced by LaSalle and Lefschetz[12]. $P$ is a positive definite matrix, $x$ is some portion of the system state, and $f(\cdot)$ is a nonlinearity which lies in sector $[0, \infty]$. That is to say

$$0 \leq f(\sigma)\sigma. \tag{6}$$

The key is to satisfy conditions such that $V \geq 0$, but

$$\dot{V} = f(z)\dot{z} + x^T P \dot{x} \leq 0. \tag{7}$$

# 5 Nonlinear Analysis of Classical Digital PLLs

The key observation in this paper is that all the digital phase detectors in Section 3 are $[0, \infty]$ sector nonlinearities for $-\pi < \theta_e < \pi$. A look at Figure 5 indicates that the phase frequency detector is a $[0, \infty]$ sector nonlinearity for all values of $\theta_e$. What this means is that with little modification, the Lyapunov redesign method on analog PLLs [1] can be directly applied to these classical digital PLLs. Rather than repeat all the examples of the previous work [1], this section will present a pair of cases to show how simply the analysis translates. The first will be the very common case of a second order loop with no zeros. Because it is a rarer case, and because the nonlinear model for a third order PLL has different stability conditions than that of the linear model [1], a third order PLL with two zeros will be presented. Similar analyses for other second and third order PLLs apply.

Also, in the cases when $P$ is a $2 \times 2$ matrix (third order PLLs) the conditions for $P > 0$ are

$$p_{11} > 0, \;\; p_{11}p_{22} > p_{12}^2, \;\; \Longrightarrow \;\; p_{22} > 0. \tag{8}$$

## 5.1 Second Order PLL with No Zeros

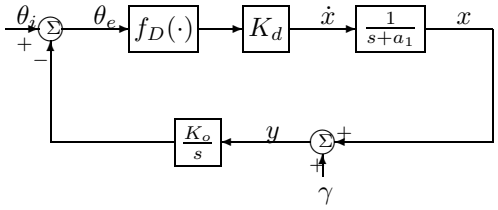


**Figure 9: Second Order Phase-Lock Loop with No Zeros**

A second order PLL with no zeros is shown in Figure 9. The differential equations corresponding to this loop with no external inputs ($\theta_i = \gamma = 0$) are:

$$\dot{x} = K_d f_D(\theta_e) - a_1 x \text{ and} \tag{9}$$

$$\dot{\theta_e} = -K_o(x + \gamma) = -K_o x, \tag{10}$$

where $\theta_e = \theta_i - \theta_o = -\theta_o$. Choose

$$V = \int_0^{\theta_e} f_D(\sigma)d\sigma + \frac{1}{2}px^2, \;\; p > 0. \tag{11}$$

The term under the integral is positive for $-\pi < \theta_e < \pi$ and this fact will be used quite often. Then

$$\dot{V} = f_D(\theta_e)\dot{\theta}_e + px\dot{x} \tag{12}$$

$$= px(K_d f_D(\theta_e) - a_1 x) + f_D(\theta_e)(-K_o x) \tag{13}$$

$$= -a_1 p x^2 + f_D(\theta_e)x(pK_d - K_o). \tag{14}$$

In order to invoke LaSalle's Theorem, we must have $V(\theta_e, x) \geq 0$ with $V = 0 \Longleftrightarrow \theta_e = x = 0$ and $\dot{V} \leq 0$. Assuming $\theta_e \in (-\pi, \pi)$ the condition for $V \geq 0$ is

$$p > 0. \tag{15}$$

The conditions that guarantee $\dot{V} \leq 0$ are:

$$a_1 p > 0, \text{ and} \tag{16}$$

$$pK_d - K_o = 0. \tag{17}$$

For $K_d, K_o > 0$ it is always possible to satisfy Conditions 17 and 15 by picking

$$p = \frac{K_o}{K_d}. \tag{18}$$

Condition 16 is easy to satisfy by picking

$$a_1 > 0, \tag{19}$$

which leaves

$$V = \int_0^{\theta_e} f_D(\sigma)d\sigma + \frac{1}{2}\frac{K_o}{K_d}x^2 \text{ and} \tag{20}$$

$$\dot{V} = -a_1\frac{K_o}{K_d}x^2 \leq 0. \tag{21}$$

For $\|x\| \to \infty$, $\|V\| \to \infty$. Finally, the only values for $\theta_e$ and $x$ which results in $\dot{V} = \dot{x} = \dot{\theta}_e = 0$ is $\theta_e = x = 0$.

### 5.1.1 Tracking a Phase Step

The second order PLL with no zeros designed above is stable. It will now be shown that this loop can also track a step input. The equations for the PLL corresponding to Figure 9 with an input at $\theta_i$ are:

$$\dot{x} = K_d f_D(\theta_e) - a_1 x, \tag{22}$$

$$\theta_e = \theta_i - \theta_o, \text{ and} \tag{23}$$

$$\dot{\theta_e} = \dot{\theta_i} - K_o(x + \gamma) = \dot{\theta_i} - K_o x. \tag{24}$$

As above, choose the Lyapunov function

$$V = \int_0^{\theta_e} f_D(\sigma)d\sigma + \frac{1}{2}\frac{K_o}{K_d}x^2, \tag{25}$$

where the choice of $p$ from Equation (18) has as been made and $a_1 > 0$. Then

$$\dot{V} = f_D(\theta_e)\dot{\theta}_i - a_1\frac{K_o}{K_d}x^2, \tag{26}$$

where the second term is the same as the no input case, Equation (21), and the first term corresponds to excitation caused by the input to $\theta_i$. Now say $\theta_i$ is a step. Then

$$\dot{\theta}_i = \theta_{i,0}\delta(t), \tag{27}$$

where $\delta(t)$ is the impulse function. Integrating (26) forward in time and noting that $f_D(\theta_e)(0^+) = \sin\theta_{i,0}$ yields (due to the sifting property of the impulse function):

$$V(t) = \int_{0^-}^{t} f_D(\theta_e)\dot{\theta}_i dt - a_1\frac{K_o}{K_d}\int_{0^-}^{t} x^2 dt \tag{28}$$

$$= \theta_{i,0}f_D(\theta_{i,0}) - a_1\frac{K_o}{K_d}\int_{0^-}^{t} x^2 dt \tag{29}$$

The first term of (29) is a positive constant for $-\pi < \theta_{i,0} < \pi$. The second term is a negative number which will grow without bound unless $x$ goes to 0. If $x$ did not converge to 0, then $V(t)$ would eventually become negative which is impossible since $V(t)$ was chosen to be a positive definite function. Thus, $x$ must converge to 0. As in the discussion of stability, the only value of $\theta_e$ for which $x$ can remain identically 0 is $\theta_e = 0$, thus the loop must track a phase step input.

## 5.2 Third Order PLL with Two Zeros

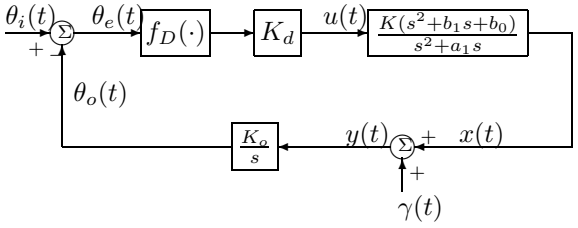


**Figure 10: Third Order Phase-Lock Loop with 2 Zeros**

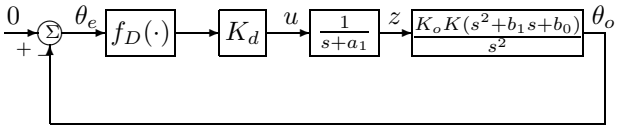


**Figure 11: Closed-Loop Nonlinear System**

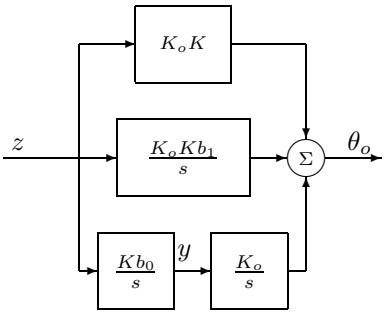


**Figure 12: Drawing out the state variables**

The block diagram of the PLL that was analyzed in full [3] is shown in Figure 10. The results will be summarized here. This is a third order PLL with two zeros. Note that an extra gain, $K$, is involve in this model, but for consistency with the previous examples this could be set to 1 without loss of generality. For the sake of stability and tracking analysis it is convenient to redraw the loop as in Figure 11. From here the necessary state variables can be drawn out as in Figure 12. The state equations corresponding to Figures 11 and 12 are:

$$\dot{z} = K_d f_D(\theta_e) - a_1 z, \tag{30}$$

$$\dot{y} = Kb_0 z, \text{ and} \tag{31}$$

$$\dot{\theta_e} = -K_oKK_d f_D(\theta_e) - K_oK(b_1 - a_1)z - K_o y \tag{32}$$

Choose

$$V = \int_0^{\theta_e} f_D(\sigma)d\sigma + \frac{1}{2}\begin{bmatrix} z & y \end{bmatrix} P \begin{bmatrix} z \\ y \end{bmatrix}, \tag{33}$$

where $P$ is a symmetric, positive definite, $2 \times 2$ ma-

trix. In order to invoke LaSalle's Theorem, we must have $V(\theta_e, y, z) \geq 0$ with $V = 0 \Longleftrightarrow \theta_e = y = z = 0$ and $\dot{V} \leq 0$. Assuming $\theta_e \in (-\pi, \pi)$ we can satisfy satisfy (8) and guarantee $V \geq 0$ and $\dot{V} \leq 0$ with:

$$P = \begin{bmatrix} \frac{K_o K}{K_d}(b_1 - a_1) & \frac{K_o}{K_d} \\ \frac{K_o}{K_d} & \frac{K_o a_1}{K_d K b_0} \end{bmatrix}, \quad (34)$$

$$K_o K K_d > 0 \Longleftrightarrow \frac{K_o K}{K_d} > 0, \quad K_d \neq 0 \quad (35)$$

$$b_1 > a_1, \ (b_1, a_1 \text{ same sign}) \text{ and} \quad (36)$$

$$b_0 - (b_1 - a_1)a_1 < 0. \quad (37)$$

It is convenient to choose both $b_0$ and $a_1 > 0$ since this corresponds to a stable filter. Also, it is convenient to choose $K_d$, $K_o$, and $K$ positive, leaving

$$\dot{V} = -f_D(\theta_e)^2 \left[K_o K K_d\right] + z^2 \left[\frac{K_o K}{K_d}(b_0 - (b_1 - a_1)a_1)\right] \leq 0. \quad (38)$$

For $\|[y \ z]\| \to \infty$, $\|V\| \to \infty$. Finally, the only place that $\dot{V}$ and (30) – (32) can vanish is for $z = y = \theta_o = \theta_e = 0$, so using LaSalle's Theorem proves stability.

### 5.3 Tracking for Third Order Loops

The tracking analysis of a step input for the third order loops is completely analogous to that of the analog PLLs [1] and the second order example in Section 5.1.1. It will be omitted here for brevity.

## 6 Conclusions

This paper has demonstrated how stability and tracking analysis for the nonlinear model of classical digital phase-lock loops, can be approached by Lyapunov redesign in a similar manner to that done by the author for analog PLLs [1]. This allows for greater confidence in these designs, particularly when the loop is out of lock. Although only a pair of examples have been presented here, it should be clear that analysis identical to the analog case can be done for all orders of classical digital PLLs, simply by replacing the $\sin(\cdot)$ nonlinearity of the phase detector with the more general $f_D(\cdot)$ nonlinearity. For a given loop design then, the range of $\theta_e$ for which the phase converges to 0 is determined by the range of $\theta_e$ over which the phase detector is a $[0, \infty]$ nonlinearity.

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