Phase-Locked Loops: A Control Centric Tutorial

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"Then I locked the phase, now I'm a believer ..."

– Shrek takes up engineering

Slides and preprint available at: http://www.labs.agilent.com/personal/Danny_Abramovitch/pubs/

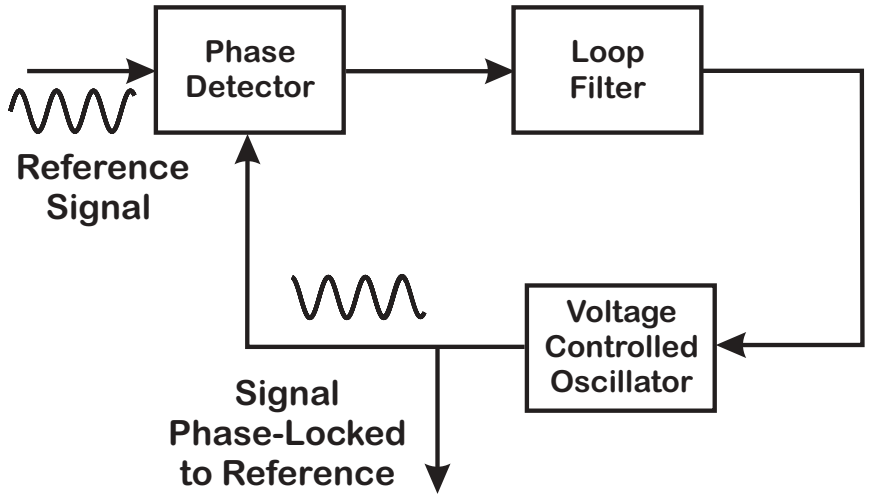
Talk Outline

- Brief History
- PLL Basics
- Linear Analysis Methods for Classical PLLs
- Nonlinear Analysis Methods for Classical PLLs
- Digital PLLs
- Loop Components
  - Phase Detectors
  - Voltage Controlled Oscillators
  - Loop Filters
- Noise
- Applications
  - PLL Applications in Control Problems
- Advanced Topics/Areas For Contribution/Useful References

An Abbreviated History of PLLs

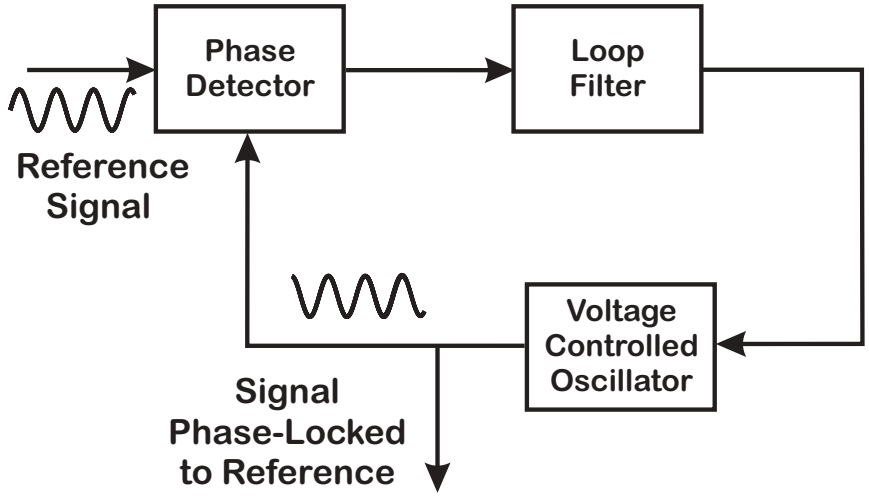
- Coincides with invention of "coherent communication" (DeBellescize, 1932).
- The earliest widespread use of PLLs to the horizontal and vertical sweeps used in television, where a continuous clocking signal had to be synchronized with a periodic synch pulse (Wendt & Fredendall, 1943). PLLs critical to development of color television (Richman, 1954).
- The first PLL IC arrived around 1965. This created an explosion in the use of PLLs.
- The first digital PLL appeared around 1970. This was of the classical digital PLL type.
- A few years later, the first all digital PLL appeared.
- The first laser appears in 1960. The first optical PLL arrives 4 years later.
- PLLs today:
  - PLLs in every cell phone, television, radio, pager, computer, all telephony, ...
  - The most prolific feedback system built by engineers.
  - At low end: all software PLLs implement entire PLL functionality on sampled data.
  - At high end: optical PLLs used in clock recovery for 160 Gbps data (OFC 2002).
  - Boy band called: N'Sync.
- So, why aren't we paying attention?
  - The field is both mature and bleeding edge.
  - Main contributions come from circuit designers.
  - They tend to be great at circuit design, but weak with filters & loop dynamics.

PLL Basics



- Basic idea of a phase-locked loop:
  - inject sinusoidal signal into the reference input
  - the internal oscillator locks to the reference
  - frequency and phase differences between the reference and internal sinusoid $\Longrightarrow k$ or 0
  - Internal sinusoid then represents a filtered version of the reference sinusoid.
  - For digital signals, Walsh functions replace sinusoids.

General PLL Block Diagram

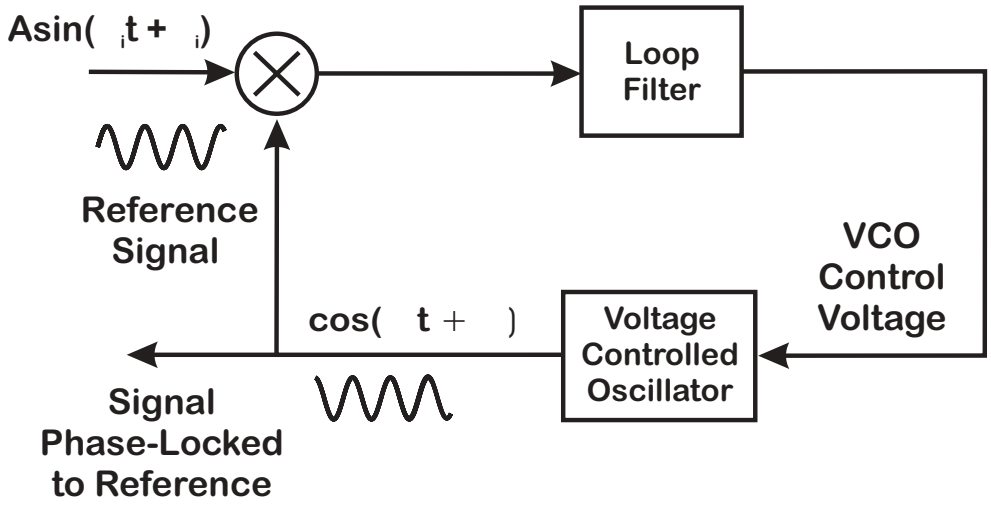


- A phase detector (PD). This is a nonlinear device whose output contains the phase difference between the two oscillating input signals.
- A voltage controlled oscillator (VCO). This is another nonlinear device which produces an oscillation whose frequency is controlled by a lower frequency input voltage.
- A loop filter (LF). While this can be omitted, resulting in what is known as a first order PLL, it is always conceptually there since PLLs depend on some sort of low pass filtering in order to function properly.
- A feedback interconnection. Namely the phase detector takes as its input the reference signal and the output of the VCO. The output of the phase detector, the phase error, is used as the control voltage for the VCO. The phase error may or may not be filtered.

Unique features of PLLs as Control Loops

- Correct operation depends on being nonlinear. Phase detector action (frequency to phase) and VCO action (phase to frequency) are nonlinear. Different parts of loop are in different spaces (signal response and phase response).
- PLLs are almost always low order (not counting various high frequency filters and parasitic poles). Typically first or second order. A few third or fourth order loops.
- With the exception of PLL controlled motors, the PLL designer is responsible for designing/specifying all the components of the feedback loop. Complete feedback loop design replaces control law design, and the designer's job is governed only by the required characteristics of the input reference signal, the required output signal, and technology limitations of the circuits themselves.
- PLL control of motors, the motor and optical coupler takes the place of the VCO. The rest is at the designer's discretion.
- Control theory used in most PLL texts is straight linear system design with a small amount of nonlinear heuristics thrown in.
- Stability analysis and design of the loops is combination of linear analysis, rule of thumb, and simulation.
- Experts in PLLs tend to be electrical engineers with hardware design backgrounds.
- General theory of PLLs and ideas on how to make them even more useful seems to cross into the controls literature only rarely.

PLL Basics



- General sinusoid at reference input can be written as:

$$v_i = R_1(t) = A\sin(\omega_i t + \theta_i). \tag{1}$$

-

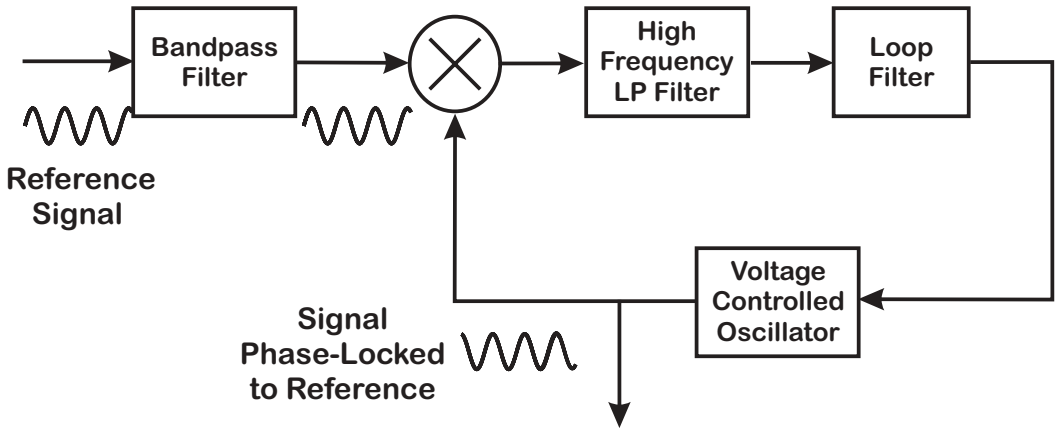
$$v_o = VCO_{out}(t) = \cos(\omega_o t + \theta_o). \tag{2}$$

- Mixer output:

$$v_d = Mixer_{out}(t) = AK_m \sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o), \tag{3}$$

where K_m is the gain of the mixer.

Typical simplifying steps:



- **Using the familiar trigonometric identity in terms of the PLL:**

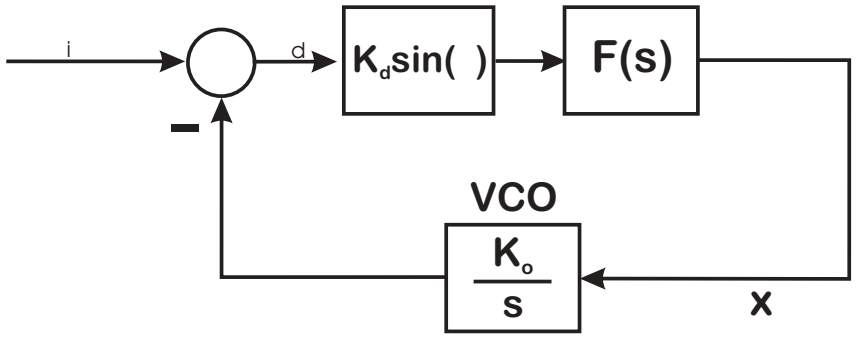
$$2\sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o) = \sin((\omega_i + \omega_o)t + \theta_i + \theta_o) + \sin((\omega_i - \omega_o)t + \theta_i - \theta_o) \tag{4}$$

- **Two fundamental assumptions lead to common analog PLL model. Let $\theta_d = \theta_i - \theta_o$. Then these assumptions are:**

  1) **The first term in (4) is attenuated by the high frequency low pass filter in and by the low pass nature of the PLL itself.**
  2) **Let $\omega_i \approx \omega_o$, so that the difference can be incorporated into θ_d. This means that the VCO can be modeled as an integrator.**
  3) **The baseband phase detector output is then:**

$$v_d(t) \approx \frac{AK_m}{2}\sin(\theta_i(t) - \theta_o(t)) = \frac{AK_m}{2}\sin(\theta_d(t)) \tag{5}$$

Standard Nonlinear Model for Analog PLLs



This is still a nonlinear system. The typical analysis methods include:

1) Linearization: For θ_d small

$$\sin\theta_d \approx \theta_d \text{ and } \cos\theta_d \approx 1.$$

Useful for studying loops that are near lock, does not help when θ_d is large.

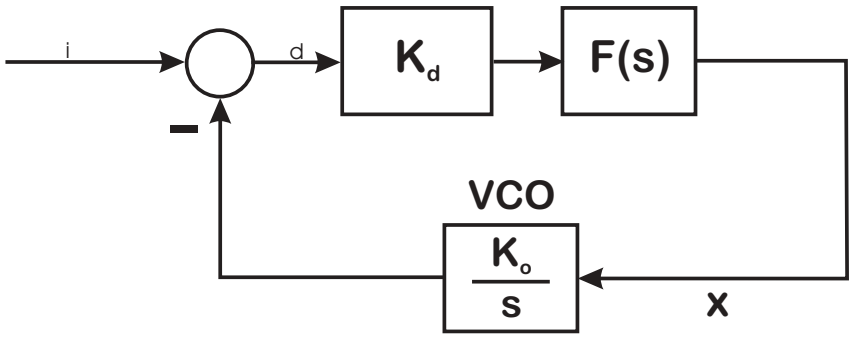
2) Phase plane portraits. Classical graphical method of analyzing behavior of low order nonlinear systems about a singular point. Can only completely describe first and second order systems.

3) Simulation. Explicit simulation of the entire PLL is relatively rare. Problem is stiff. Simulations that sample fast enough to characterize the $2\omega_o t$ term are often far too slow to effectively characterize the baseband.

$\Longrightarrow$ Simulate the response of the components (phase detector, filter, VCO) in signal response space.

$\Longrightarrow$ Simulate the entire loop only in signal phase space.

Standard Linear Model for Analog PLLs



Used for most analysis and measurements of PLLs. Model has some omissions:

1) The texts typically omit the input bandpass filter.

- Not in the loop itself & the actual input frequency is often not known or is variable.
- The designer has some idea of the range of the signal.
- Input bandpass filter can considerably reduce broadband noise entering the system.

2) The texts typically omit the high frequency low pass filter. The loop filter is optimized for the stability and performance of the baseband (phase).

3) Amplitude of the phase error is dependent upon A, the input signal amplitude. The linearized model has a loop gain that is dependent upon the loop components. Thus, in practical loop design, the input amplitude must either be regulated or its affects on the loop must be anticipated.

Linear Analysis for Classical PLLs

- **Transfer function from reference (input) phase to oscillator (clock) phase**

$$T(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d F(s) K_v / s}{1 + K_d F(s) K_v / s} = \frac{K_d K_v F(s)}{s + K_d K_v F(s)}$$

- **Transfer function from reference phase to phase error**

$$S(s) = \frac{\theta_d(s)}{\theta_i(s)} = \frac{1}{1 + K_d F(s) K_v / s} = \frac{s}{s + K_d K_v F(s)}$$

- **Hold Range: the frequency range over which the PLL is able to statically maintain phase tracking:**

$$\Delta\omega_H = K_o K_d F(0).$$

- **Lock Range: the frequency range within which the PLL locks within one single-beat note between the reference frequency and output frequency:**

$$\Delta\omega_L \approx \pm K_o K_d F(\infty).$$

- **The Pull-In and Pull-Out Range:**
  The pull-in range, $\Delta\omega_P$, is defined as the frequency range in which the PLL will always become locked. The pull-out range, $\Delta\omega_{PO}$, is defined as the limit of dynamic stability for the PLL. No simple relationships for these.

The Steady-State Error via the Final Value Theorem

$$\begin{aligned}\lim_{t\to\infty}\theta_d(t) &= \lim_{s\to 0} s\theta_d(s)\\ &= \lim_{s\to 0} s\theta_i(s)S(s)\end{aligned}$$

- VCO as integrator makes every PLL at least Type 1
  - Zero steady state error to a phase step.
- Most PLL designs are second order, with integrator and minimum phase zero in the filter $\Longrightarrow$ Type 2 systems.
  - Zero steady state error to a phase ramp.
- Third order and higher PLL designs are not that common.
  - Few applications need zero steady state error for an accelerating phase (e.g. deep space communications with Doppler shift).
  - Stability bounds for nonlinear third order system are not the same as stability bounds for third order linear system.

  Many PLLs have high frequency filters or parasitic capacitances, but these are well beyond the loop bandwidth.

Nonlinear Analysis Methods for Classical PLLs

- **Phase Plane**
  - Analyze the second order equation:

$$\frac{d^2\phi}{d\tau^2} + \frac{\lambda d\phi}{d\tau} - \cos\phi = -\nu$$

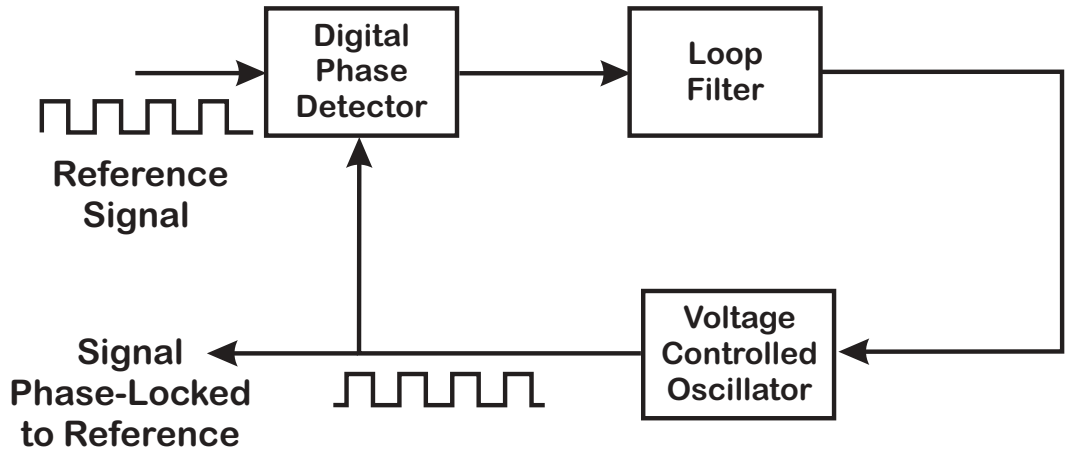
  - Classical nonlinear systems analysis method, but limited to first and second order systems.
    $\Longrightarrow$ Another reason why third order loops are avoided
- **Lyapunov Redesign**
  - Construct energy function as:

$$V = \int_0^{\theta_d} \sin(\sigma) d\sigma + \frac{1}{2} \begin{bmatrix} x_1 & x_2 \end{bmatrix} P \begin{bmatrix} x_1 \\ x_2 \end{bmatrix},$$

    where the x_i are the internal states of the PLL, θ_d is the error signal at the phase detector, and the elements of P are chosen to satisfy LaSalle's theorem.
  - Generally useful for analog PLLs and classical digital PLLs (2003).
  - Sampling of all digital PLLs makes analysis a lot harder.
  - Not limited to any order PLL, but becomes unwieldy at higher orders
- **Circle/Popov Criteria**
  - Paper by Eva Wu in 2002 ACC.

Digital Signals

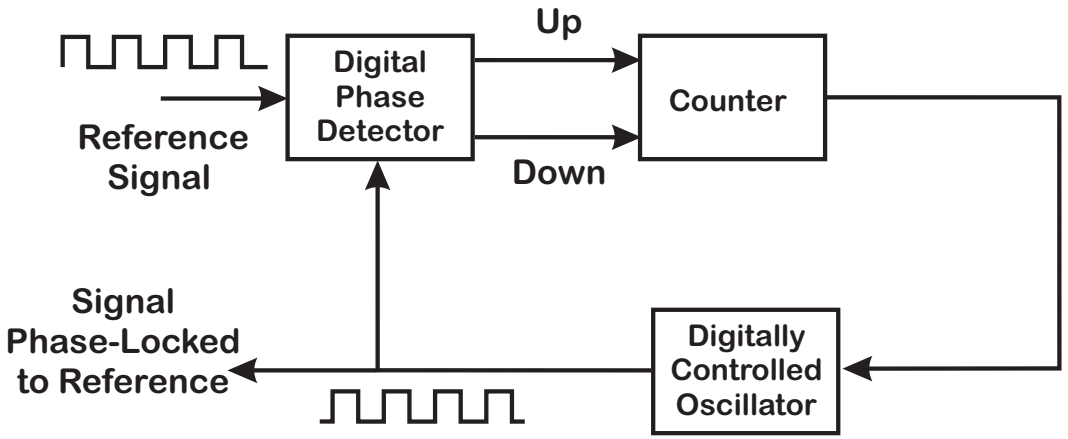
- Replace analog voltages by digital logic levels
- One or more components replaced by a digital counterpart
- Common for clock signals and digital communications
- Important feature of digital PLLs:
  - Most digital phase detectors are linear in phase over some region.
  - Thus linear analysis is fairly accurate.



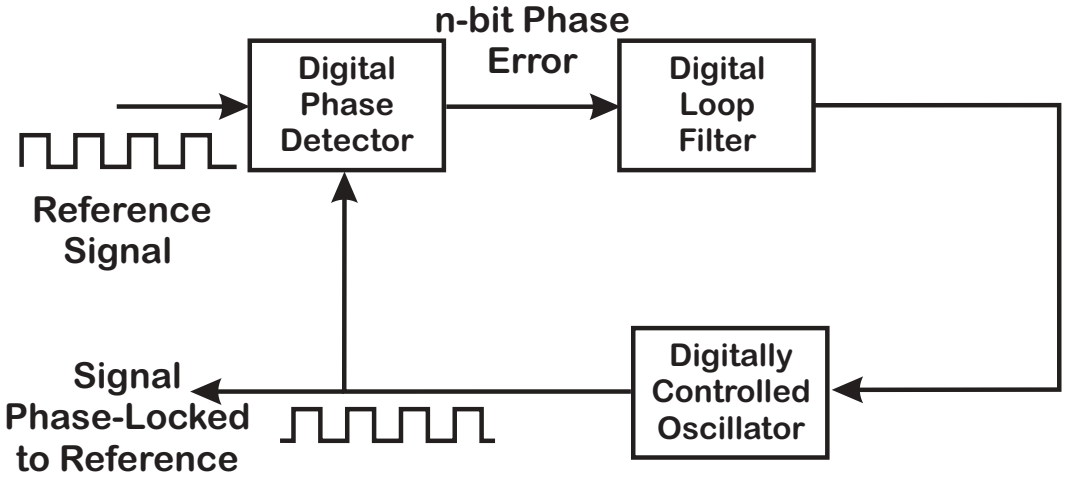
Classical Digital PLL

- The phase detector is digital, working with binary values.
- The filters and VCO are analog.
- One interpretation:
  - Signal space is digital.
  - Signal phase space is analog.

All Digital PLLs

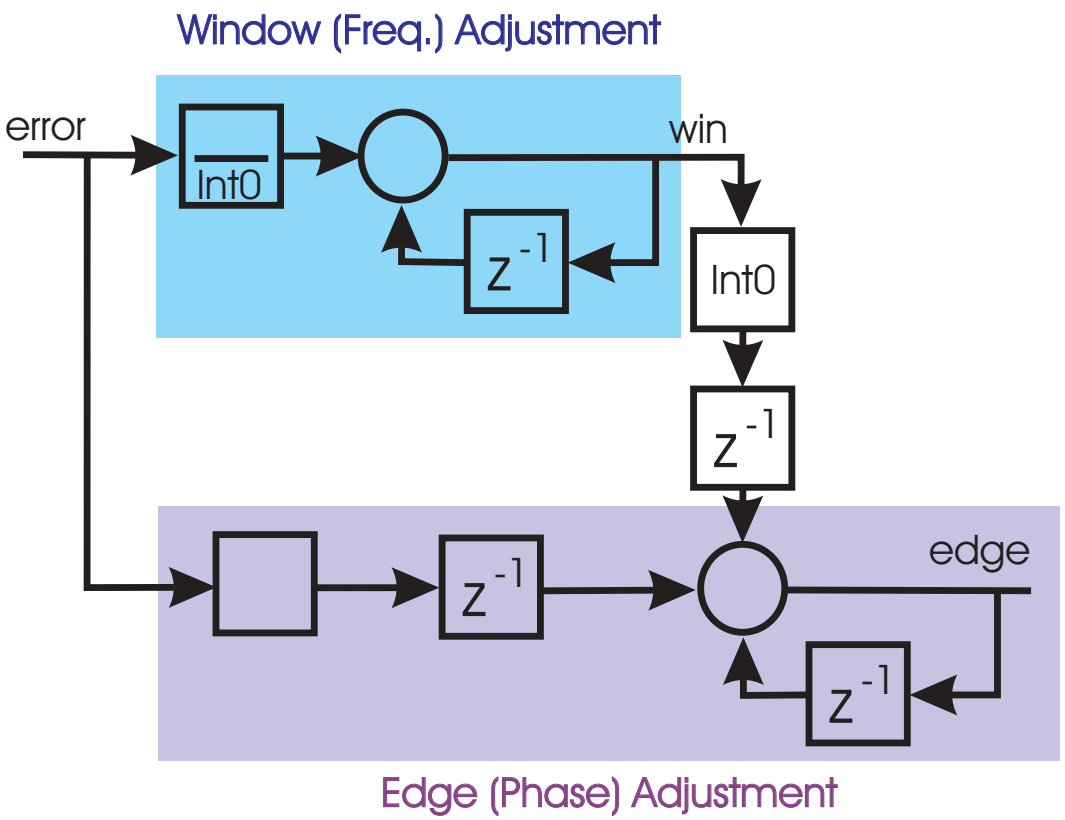


- An all digital phase locked loop.
- The digital phase detector produces pulses that go into the count up or count down inputs of the counter, which acts as the loop filter.
- The counter then adjusts the frequency of the digitally controlled oscillator (DCO).



- Another all digital phase locked loop.
- The digital phase detector produces samples of phase error in an n-bit value.
- This value is fed to a digital filter whose output adjusts the the frequency of the digitally controlled oscillator (DCO).

Software PLLs



- An example of a software PLL that does clock/data recovery.
- This heuristic loop uses a zero crossing detector on the sampled input.
- The effective sample rate is derived from the average bit zero crossing rate.

When data can be sampled at a rate substantially faster than the loop center frequency, the entire loop operation can be implemented in software. This has the advantage of flexibility. Any type of PLL can be implemented in software provided the sample rate is high enough. Software loops have a lot in common with simulation. One key difference is that the software loops deal with real data. Software PLLs may operate on the data in real time, but can also be used in the post processing of measured data. One cautionary note is that certain operations which are highly effective in hardware, such as limiters which have a lot of high frequency content, create real sampling issues for software loops.

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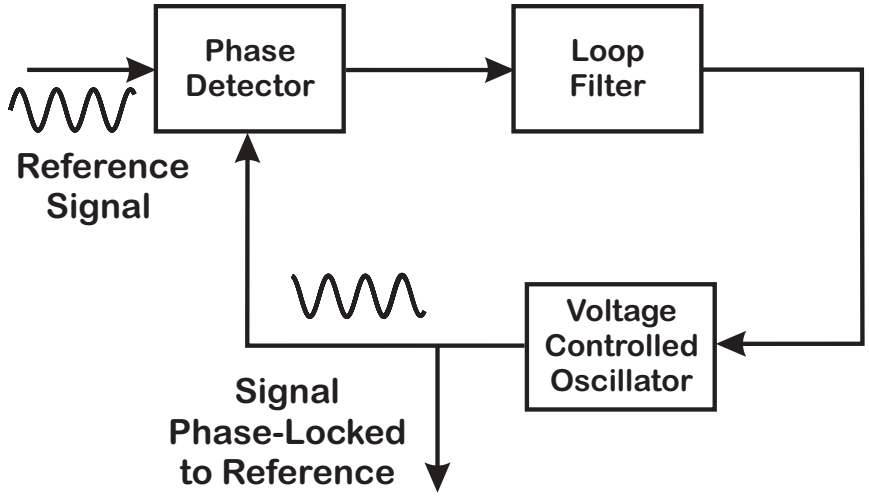
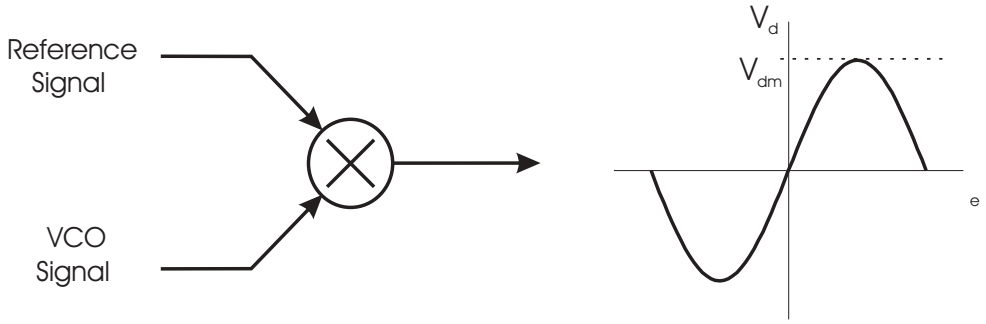
Phase Detectors

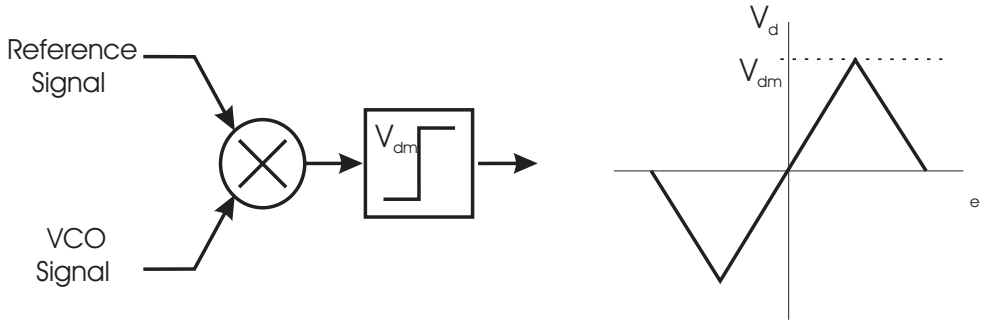


- Whether or not a PLL can track a signal is largely dependent on the phase detector.
- This is the usual starting point for any PLL design.
- Phase detector analysis is largely accomplished by drawing square wave diagrams and then drawing conclusions about the baseband behavior.
- This is annoying to servo people, but it works.
- Drawing your own diagram is the only way to understand the workings of a phase detector.

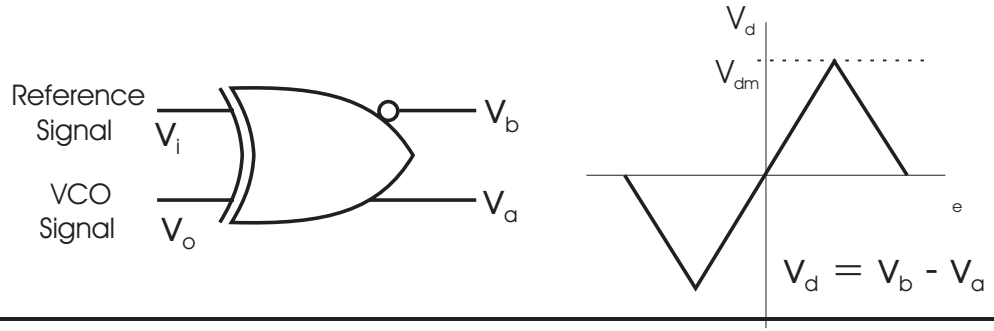
Phase Detectors (memoryless)



- Classical mixing phase detector

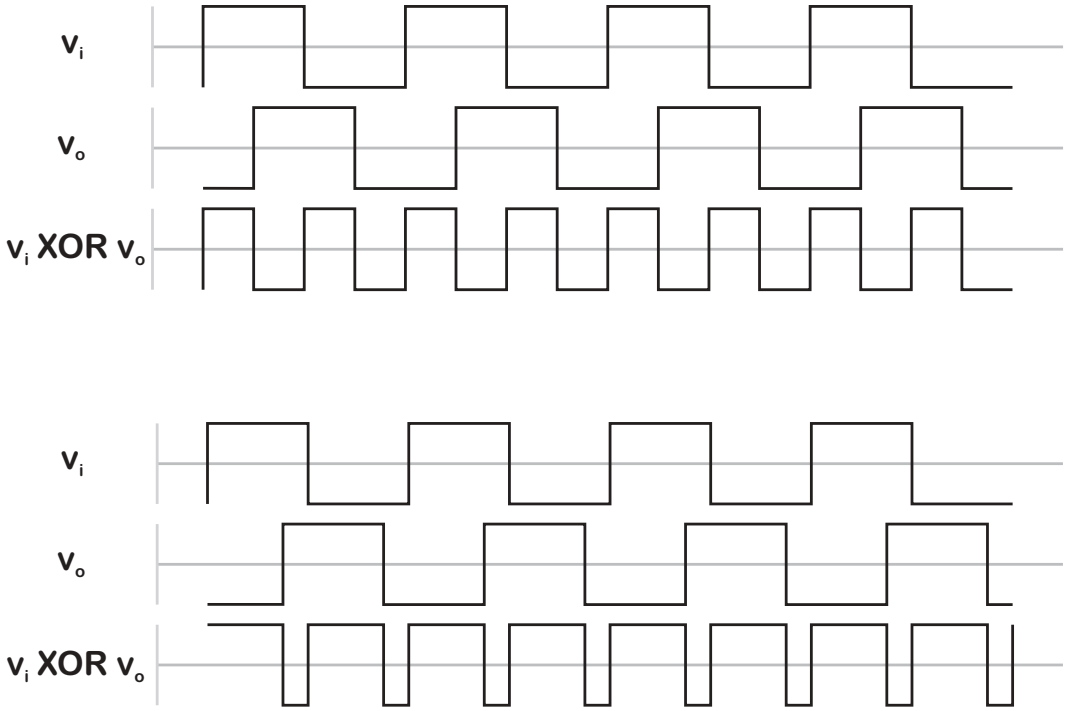


- An over driven mixing phase detector.
- As the mixer saturates, the outputs depend on the effective logical states of the input signals.
- It starts to behave like an XOR.
- This is also a way to implement very high speed XORs.



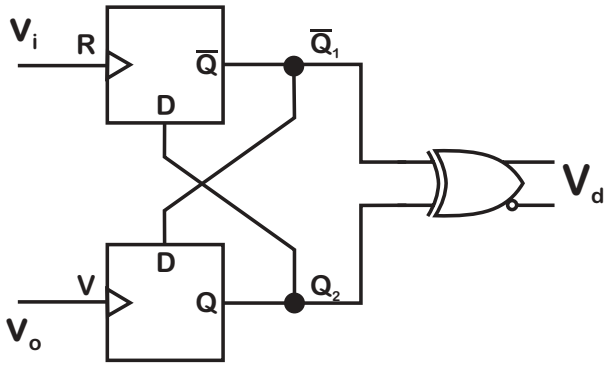
- Phase detection using an XOR gate.
- Note that this accomplishes the same thing as an over driven mixer, but with digital circuitry.

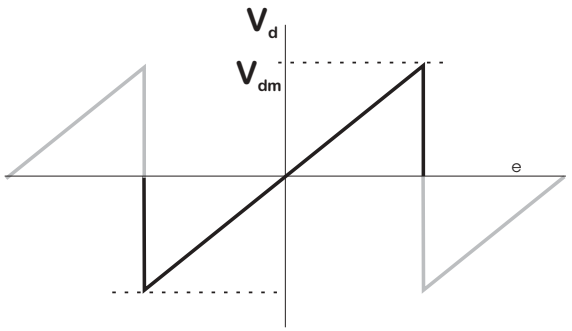
XOR Phase Detector (Analysis)



- Analysis via square wave drawings.
- XOR response can be split into a 2X term and a residual term.
- The average of the residual term is the "baseband" that we care about.
- Integrating over N clock periods drives out the 2X term.
- A phase shift of $\pi/2$ produces a residual of 0.
- A phase shift of $\pi/4$ produces a nonzero residual.
- This is how most phase detectors are analyzed.
- In fact, the analog voltages contain many harmonics. In designing frequency synthesizers, much effort is spent keeping these harmonics from modulating the VCO.

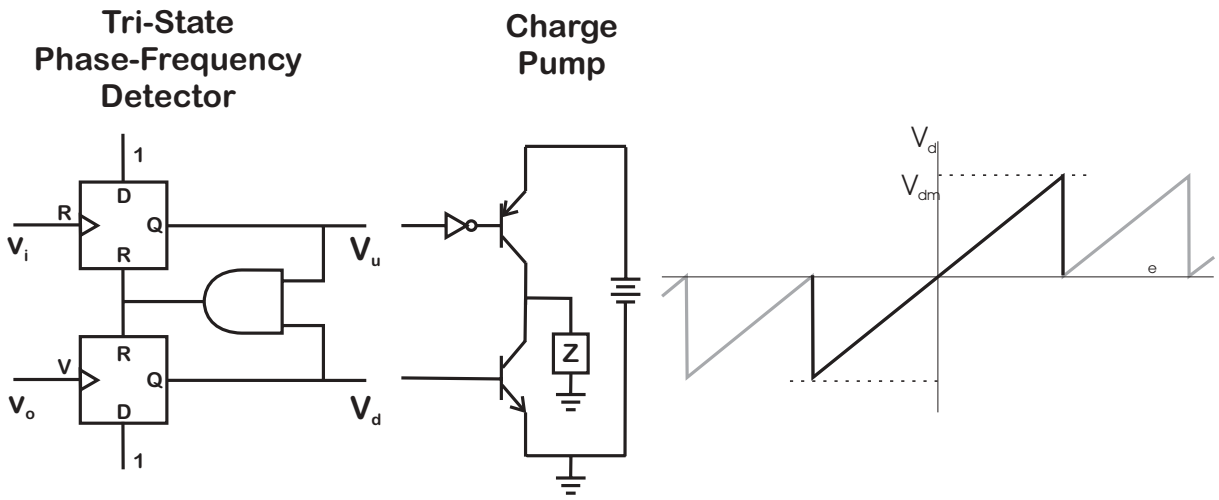
A 2 State Phase Detector





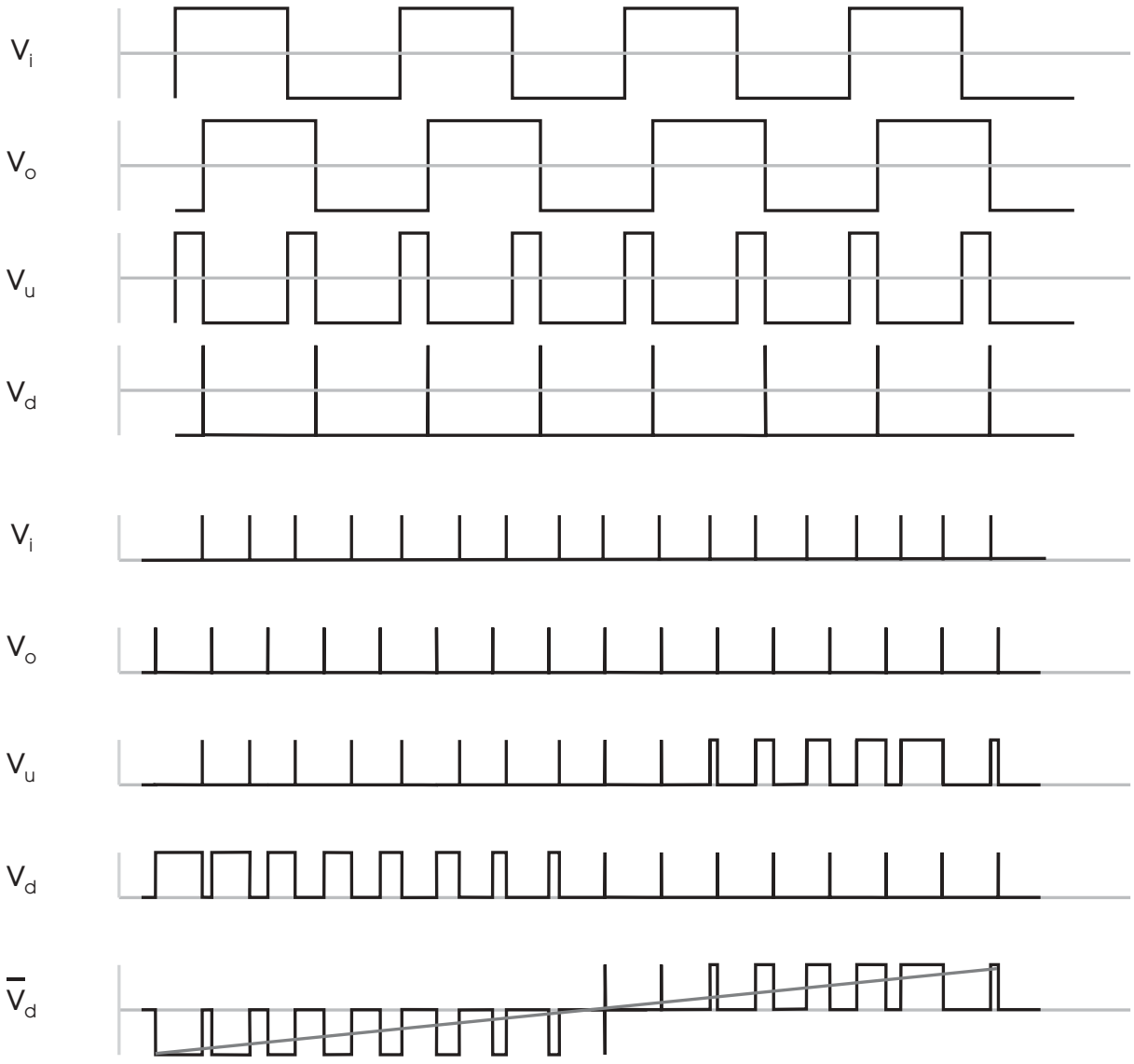
- Two state phase detection using flip-flops as well as gates.
- The addition of the flip-flops adds memory to the system.
- The flip-flops are typically sensitive to only one clock edge
  $\Longrightarrow$ only the leading edges of the input and oscillator signals matter, not their duty cycles.
- The characteristic is a sawtooth.
- The memory elements desensitizes the PD to duty cycles, but makes it more sensitive to noise.

Phase-Frequency Detector



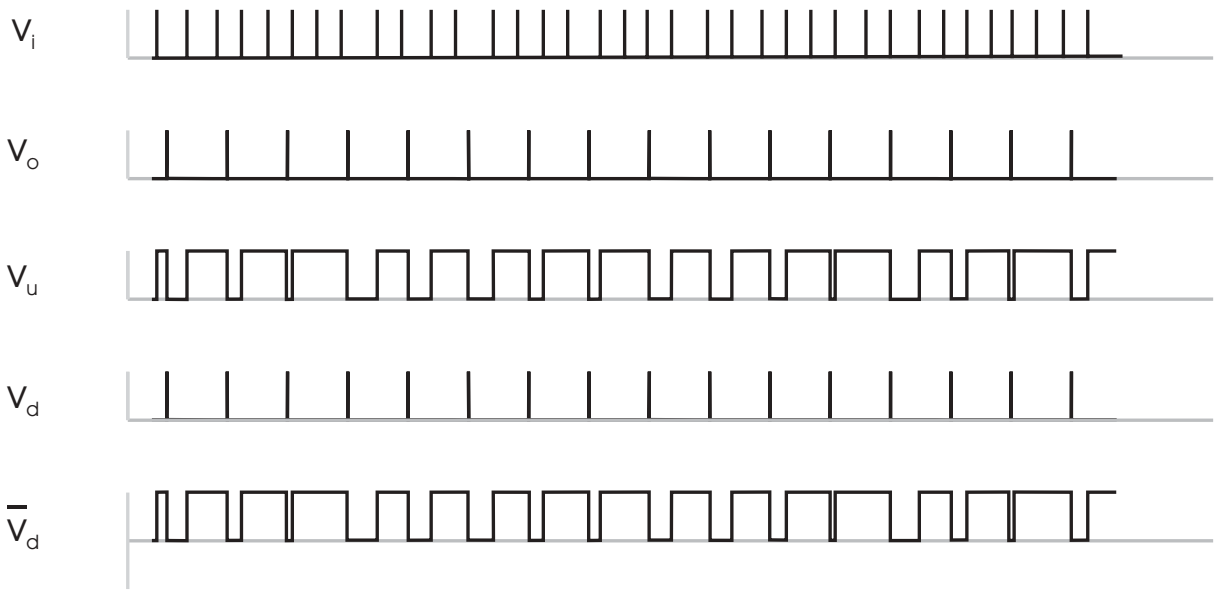
- The combination of a tri-state phase-frequency detector and a charge pump.
- The charge pump can be viewed as a 3 position switch controlled by the phase-frequency detector.
- The action of the charge pump is to alleviate any loading of the phase detector in driving the rest of the circuit. This allows the response to be smoother than without the charge pump.
- An extremely popular phase detector. Used in frequency synthesis, motor control, etc.
- Note that the loop filter is often implemented in the Z block of the charge pump.
- Note that the 4π linear range is due to memory. PD can come up in one of 2 possible states and the PLL must account for this.

Phase-Frequency Detector (Analysis)

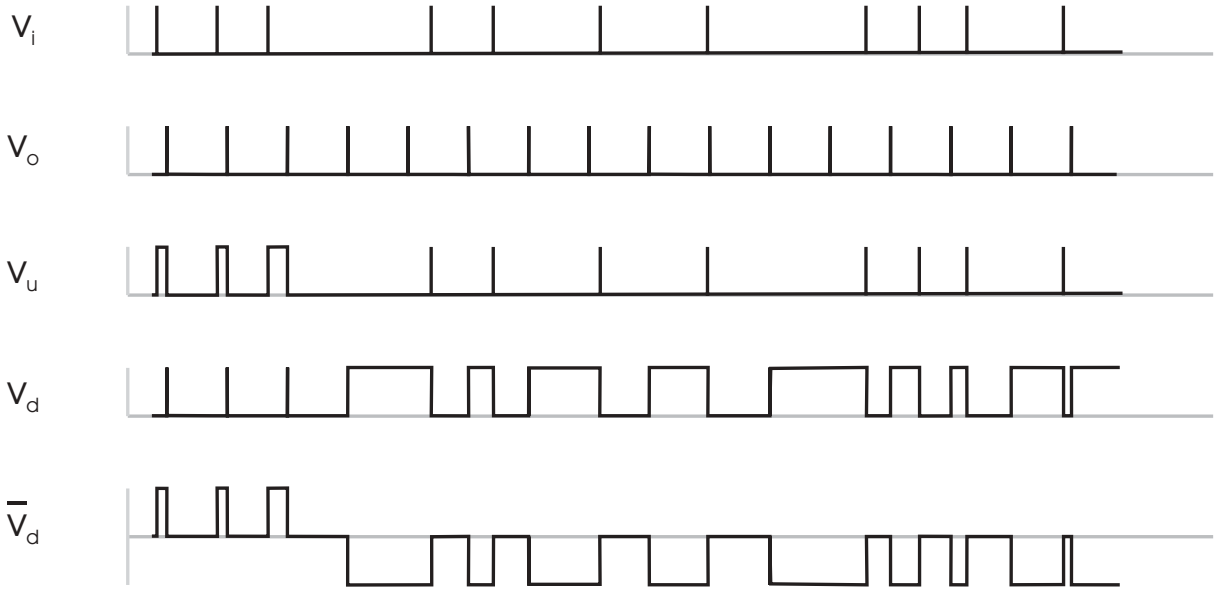


- A small phase difference shows that only the leading edges of the signal and not the duty cycle are important.
- As only the leading edges are significant, these are compared to show the phase behavior of the detector.

Phase-Frequency Detector Applications

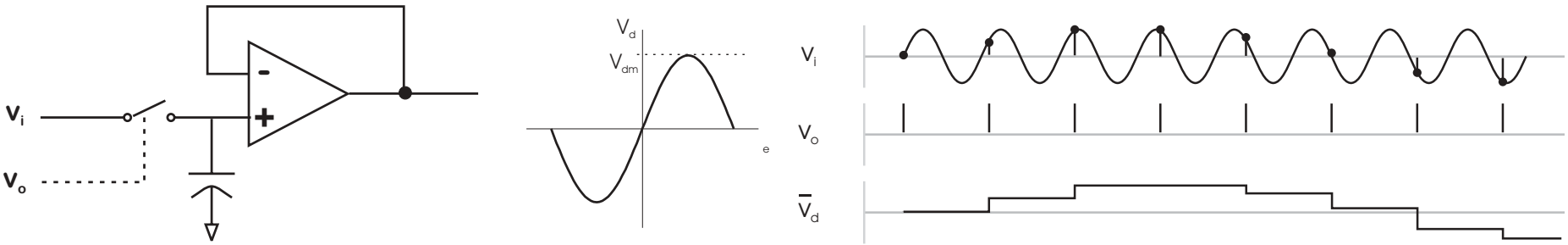


- This diagram shows how the PFD responds to frequency errors.
- The response rapidly slews the frequency towards the correct value (albeit in a nonlinear fashion).



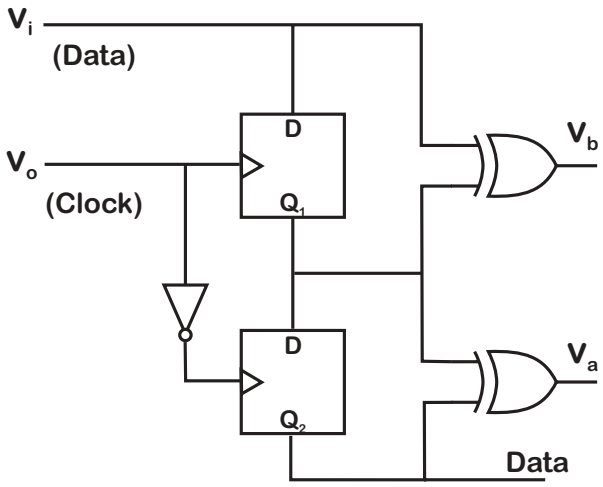
- This same property makes the PFD ineffective for use in clock data recovery (CDR).
- The "missing" transitions in the data trick the PFD into slewing the frequency to a lower clock rate, as shown in the right diagram.

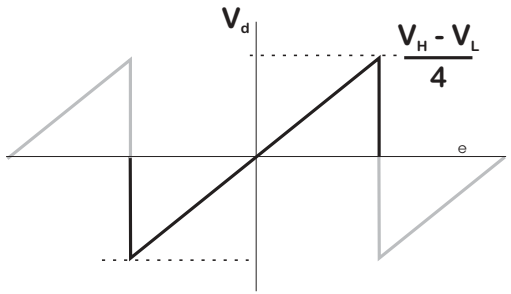
Sample and Hold Phase Detector



- The input signal, v_i is sinusoidal as shown in the right top plot.
- The VCO signal, v_o is used to trigger sampling of v_i as shown in the right middle plot.
- If the frequency of v_o matches or is close to the input frequency, the value of the sampled signal will depend only on the relative phase of v_i and v_o.
- Because the sample rate is below the Nyquist frequency, the samples alias down.
- These aliased samples create a phase error signal as seen in the right lower plot.
- The shape of the phase detector characteristic is based on the shape of the input signal, v_i, so that if v_i is sinusoidal, $\bar{v}_d$ is sinusoidal. If v_i is triangular, $\bar{v}_d$ is triangular. Finally, if v_i is a square/rectangular, then $\bar{v}_d$ has a relay characteristic.
- Note also that there is no high frequency component resulting from this phase detector. This can be seen analytically due to the fact that the zero-order hold has a zero at the sample frequency.

A Linear Clock Phase Detector

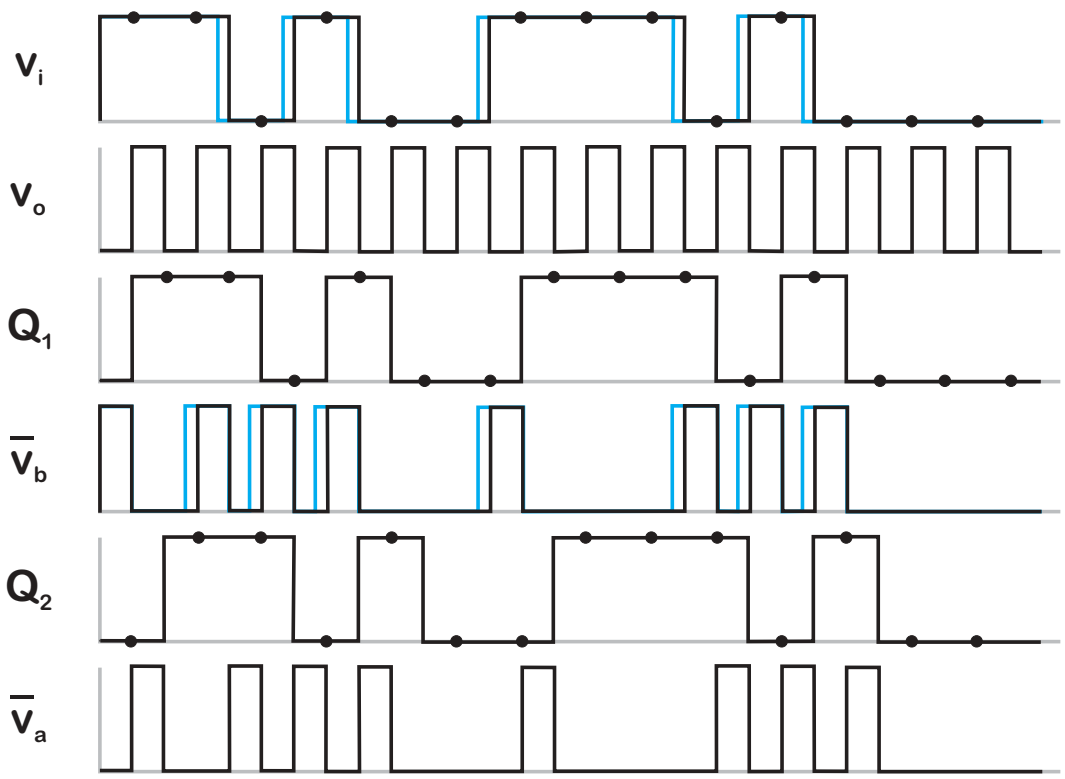




For 50% transition density.

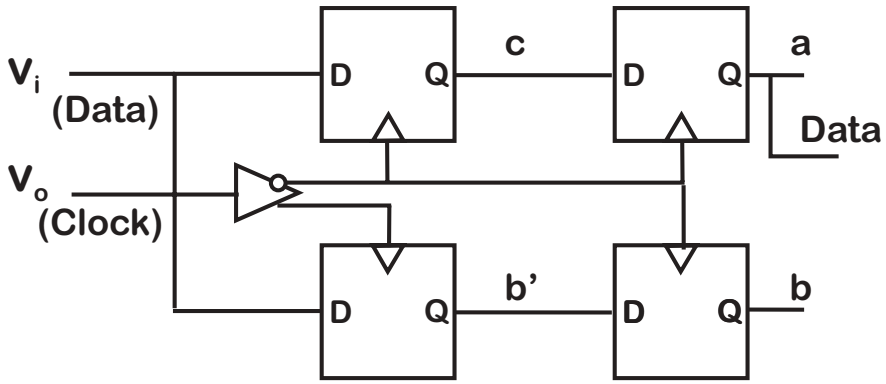
- The Hogge phase detector (Hogge, 1985).
- Used primarily in clock data recovery applications (CDR), the Hogge detector has a linear characteristic.
- XOR output $\bar{V}_b$ generates pulses where the leading edge is controlled by the data timing and the trailing edge is controlled by the clock.
- Both edges of $\bar{V}_a$ are controlled by the clock.
- So $\bar{V}_b$ is modulated by the signal phase while $\bar{V}_a$ is not.
- The difference gives a phase error for the data signal.

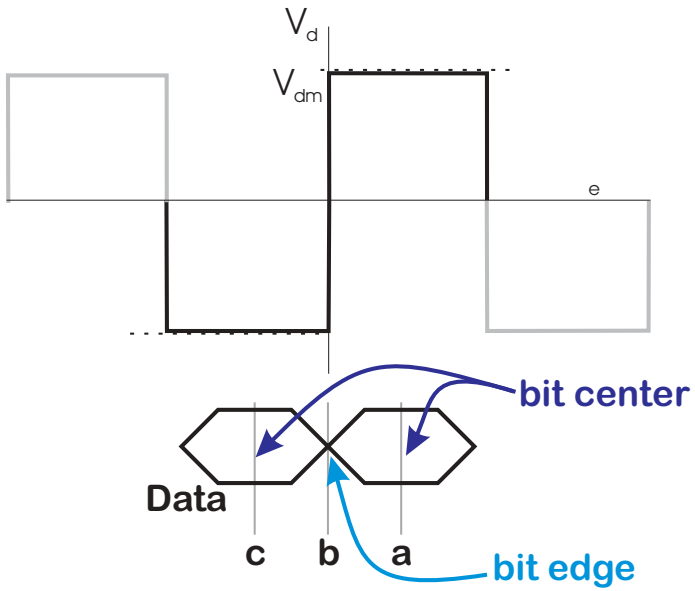
Operation of the Hogge Phase Detector



- V_i is data signal
- V_o is oscillator output (clock)
- Q_1 and Q_2 are retimed versions of V_i
- XORS give the following behavior:
  - V_b is XOR of data signal and retimed data
  - V_a is XOR of Q_1 and $Q_2 \Longrightarrow$ not modulated by phase
- avg$(V_b - V_a)$ is linear with phase difference between data and clock

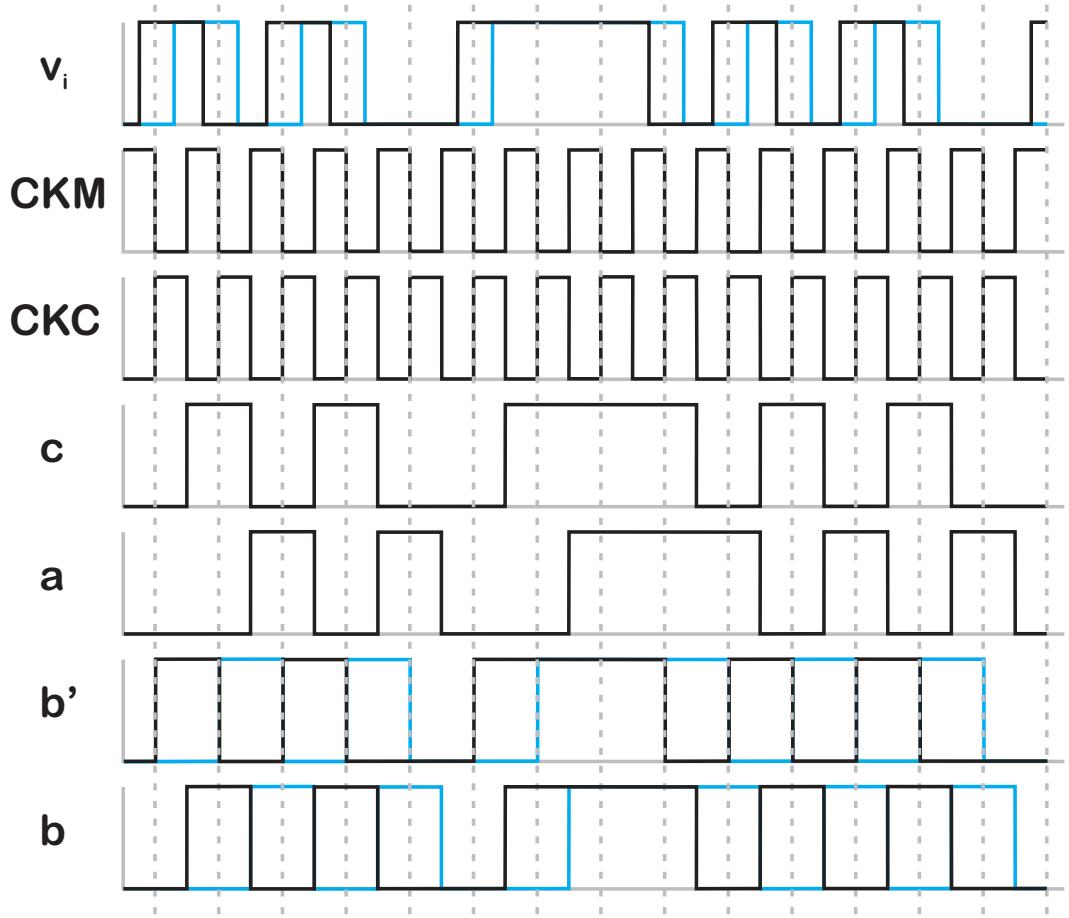
Bang Bang Phase Detector





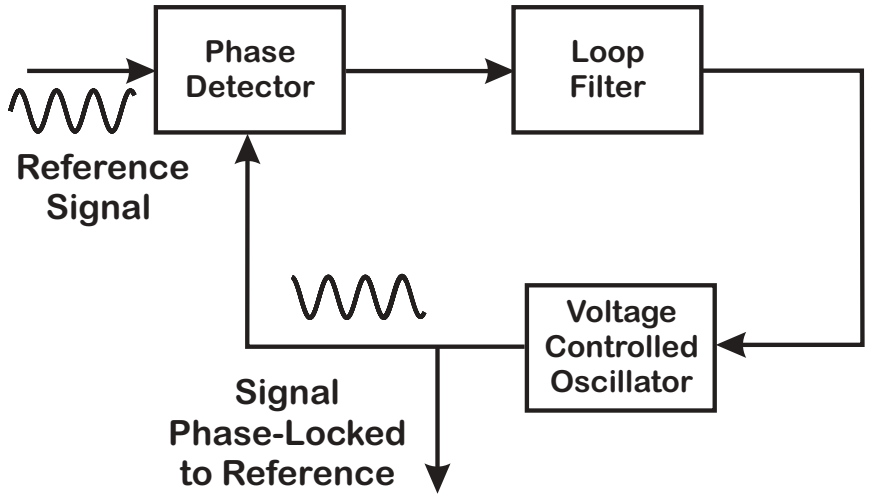
- The Alexander (Bang-Bang) phase detector.
- On the left is the original version made of component flip flops.
- The Bang-Bang phase detector is unique among the detectors presented here in that its baseband behavior is never linear.
- Instead, the detector acts as a relay over the region from $-\pi$ to π (on the right).
- Nonlinearity is a bad thing, but this is highly manufacturable for extremely high speed circuits.
- Analogous to Bang-Bang control.

Operation of the Bang-Bang Phase Detector



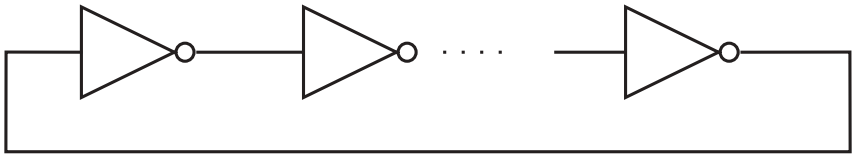
- The signals a, b, and c are re-timed versions of the data signal.
- a and c are one bit period apart, b is sampled at the half period between a and c.
- Basically, if a and c are the same, then no transition has occurred and the output of the phase detector is tri-stated.
- If not, then the state depends on b.
- If b = a, then the clock is early.
- If b = c, then the clock is late.

Voltage Controlled Oscillators (VCOs)

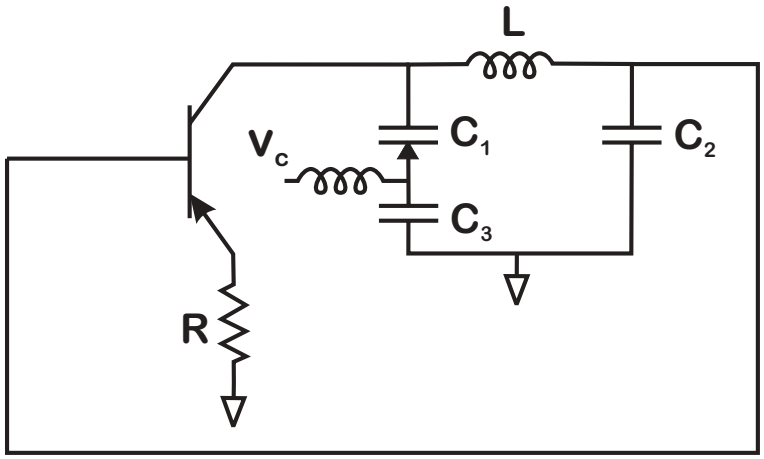


- The cleanliness of the output clock is largely determined by the VCO.
- People make careers out of doing VCO design and analysis of VCO noise.
- This corresponds to the pendulum portion of a mechanical clock.

Voltage Controlled Oscillators

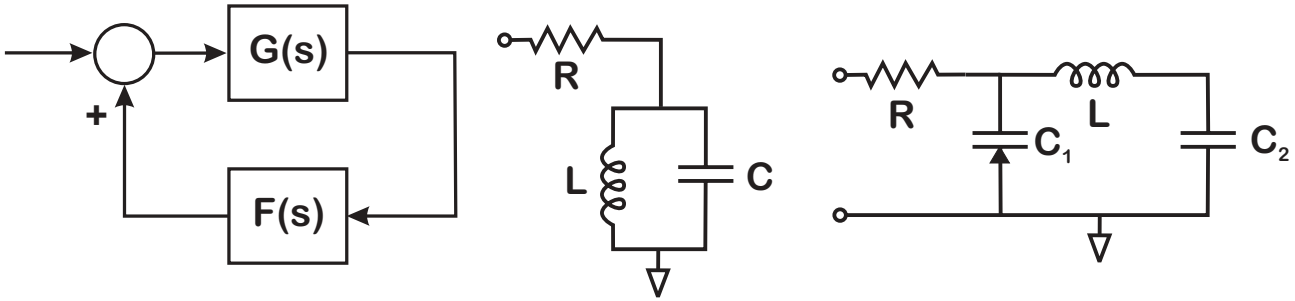


- Actual clock from PLL is the VCO output.
- VCO's frequency is modulated by input voltage.
- Ring Oscillator: common in monolithic topologies uses an odd number of inverters connected in a feedback loop.
- Relaxation Oscillator: uses a Schmitt-trigger to generate a stable square wave.
- Resonant Oscillator: puts a resonant circuit in the positive feedback path of a voltage to current amplifier. The amplifier is voltage to current amplifier with close to unity gain. The resonant circuit in the positive feedback path has poles close to the $j\omega$ axis.



- The frequency is controlled by altering the capacitance of the resonator, typically by using a varactor diode as a capacitor.
- Other forms of VCOs, such as crystal oscillators and YIG oscillators essentially run on the same principle, but modify the resonant circuit.

Resonant Oscillator VCOs



- On the left, a block diagram of an oscillator implemented as a positive feedback loop between a voltage to current amplifier through a resonant circuit.
- On the right, examples of resonant circuits: a LC tank and a π network.
- Resonant filter:

$$F(s) = \frac{2\zeta\omega_0 s}{s^2 + 2\zeta\omega_0 s + \omega_0^2},$$

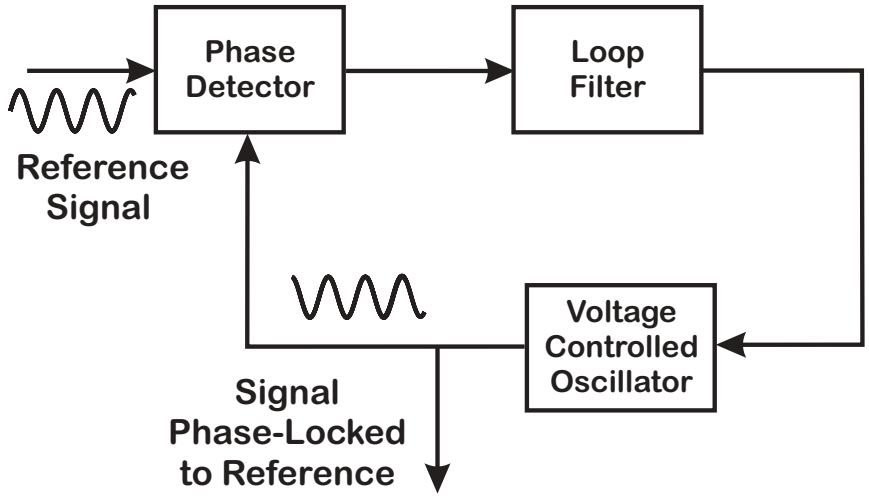
- For $G(s) = K < 1$

$$VCO(s) = \frac{G(s)}{1 - G(s)F(s)} = K\frac{s^2 + 2\zeta\omega_0 s + \omega_0^2}{s^2 + 2\zeta_1\omega_0 s + \omega_0^2},$$

  where $\zeta_1 = (1 - K)\zeta$.

- The lowering of the damping ratio is called "Q multiplication" ($Q = \frac{1}{2\zeta}$) and moves the poles even closer to the $j\omega$ axis.
- In the case of the π network, there is a complex pair of poles and one pole on the negative real axis. The dominant effect, Q amplification, takes place on the complex pair.

Loop Filter

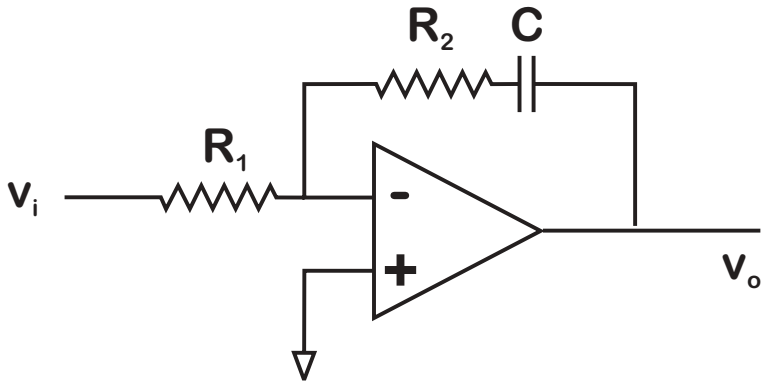


- The loop filter is the one place where the designer really gets to shape the loop.
- Unfortunately, most filters are first order.

$\Longrightarrow$ Not many degrees of freedom here.

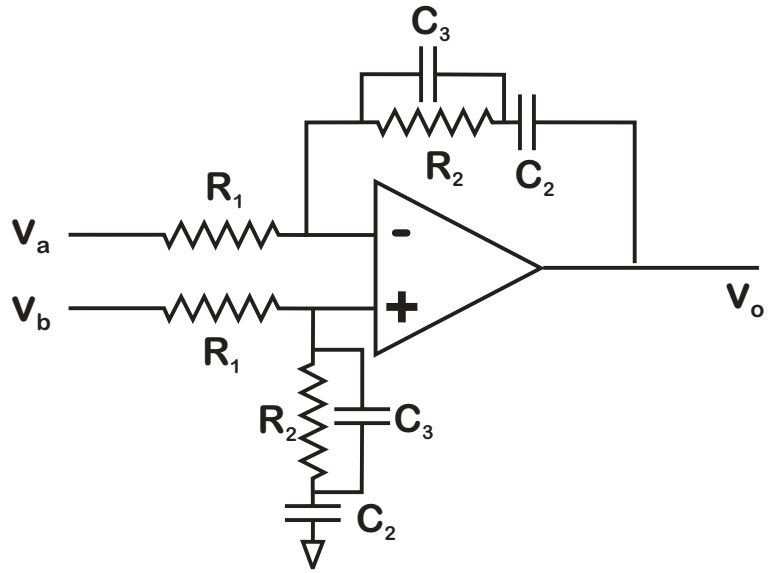
- This is where (as a rule) circuit designers seem to fall apart.

Analog Loop Filters



- First order, single ended input.
- Filter transfer function:

$$\frac{V_o}{V_i} = -\frac{sR_2C + 1}{sR_1C}.$$



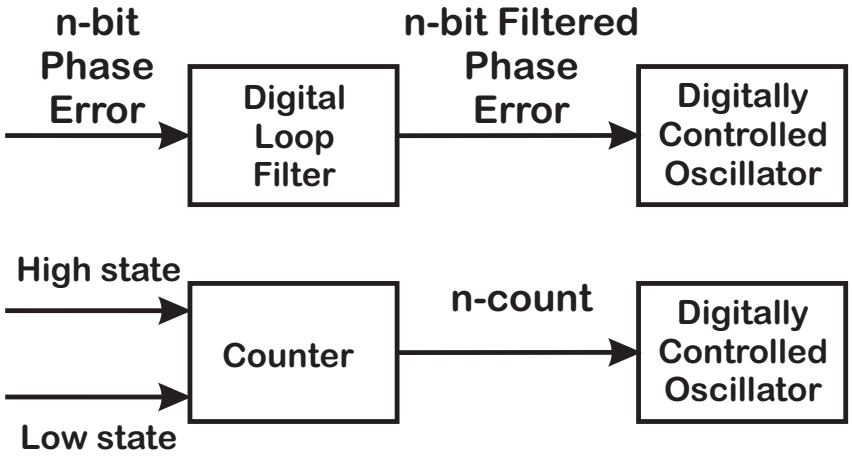
- Analog loop filter for differential inputs.
- Filter transfer function:

$$\frac{V_o}{V_a - V_b} = -\frac{sR_2(C_2 + C_3) + 1}{sR_1C_2(sR_2C_3 + 1)}.$$

- For a typical second order loop, we let $C_3 = 0$.
- For single ended input, simply tie the positive terminal of the op-amp to ground.

- For tutorial purposes only. Real implementation is different.

Digital Loop Filters



- When phase detector gives n-bit number, can use standard digital filter.
- When phase detector gives pulses, filter is often implemented as some type of counter.

Example of counter filter:

- DCO center frequency set for nominal counter value, N
- up/down pulses add to/subtract from N
- counter output is an average of the PD pulses:

$$n_{out}(z) = (1 + z^{-1} + z^{-2} + z^{-3} + \ldots)\theta_d(z),$$

$\Longrightarrow$ digital integrator with a zero at z = 0.

- Equivalent transfer function:

$$\frac{n_{out}(z)}{\theta_d(z)} = \frac{1}{1 - z^{-1}} = \frac{z}{z - 1}.$$

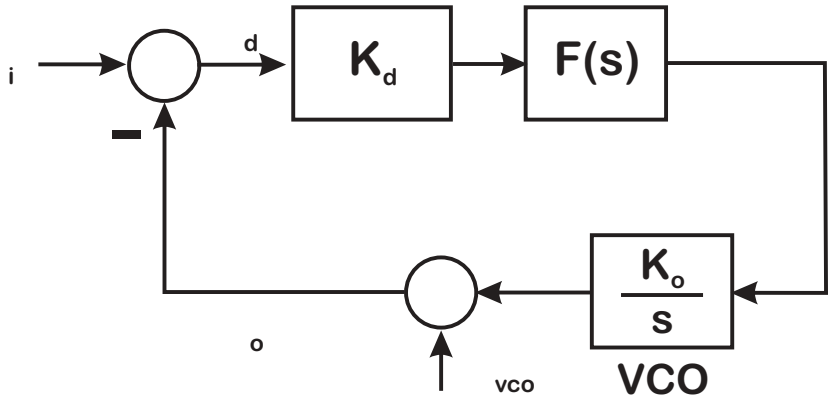
- PLL open loop is:

$$\frac{\theta_{out}(z)}{\theta_d(z)} = \frac{K_d K_v T}{2} \frac{z(z+1)}{(z-1)^2},$$

$\Longrightarrow$ poles stay in unit circle.

- Large excess in up or down pulses saturates the counter in one direction or another $\Longrightarrow$ lowers the effective loop gain but does not destabilize loop.

Simplified Noise Analysis



- Linear model of input and VCO noise passing through a PLL.
- Noise in output phase, θ_o, is one of the key performance measures of a PLL.

Extremely simplified view of phase noise. That's another tutorial.

- Output phase as a function of inputs:

$$\theta_o = T(s)\theta_i + S(s)\theta_{vco}$$

- Assuming θ_i and θ_{vco} are independent, the PSD of the output phase is given by:

$$G_{oo}(j\omega) = \|T(j\omega)\|^2 G_{ii}(j\omega) + \|S(j\omega)\|^2 G_{vv}(j\omega).$$

- Within loop bandwidth, designer has some control over the effect of θ_i on θ_o through the shaping of the loop, but beyond the loop bandwidth, θ_o is dominated by θ_{vco}.
- Every component of PLL is a potential noise source:

$\Longrightarrow$ There are noise inputs all around the loop.

$\Longrightarrow$ People make careers out of modeling the input noises.

Talk Outline

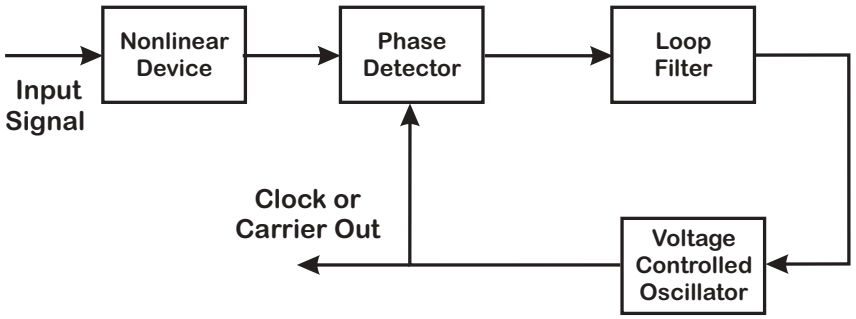
- Brief History
- PLL Basics
- Linear Analysis Methods for Classical PLLs
- Nonlinear Analysis Methods for Classical PLLs
- Digital PLLs
- Loop Components
  - Phase Detectors
  - Voltage Controlled Oscillators
  - Loop Filters
- Noise
- Applications
  - PLL Applications in Control Problems
- Advanced Topics/Areas For Contribution/Useful References

A Sample of PLL Applications

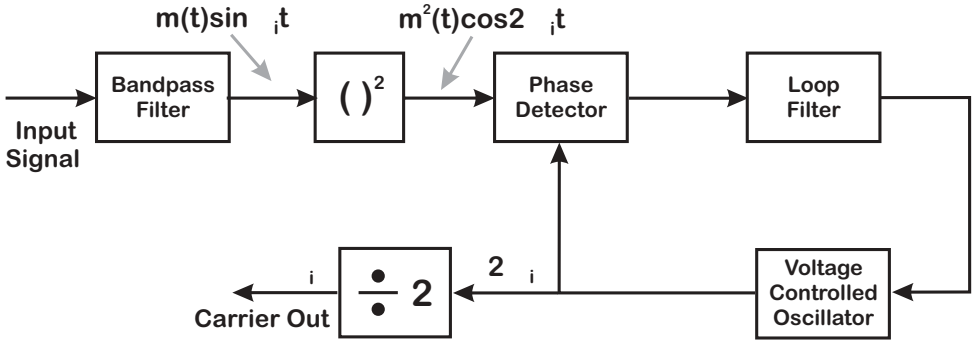
The reason that PLLs are so ubiquitous is that they are so useful in so many applications.

- Carrier Recovery
- Costas Loop
- Clock/Data Recovery
- Frequency Synthesis
- Modulation/Demodulation
- PLL Applications in Control Problems
  - Disk Drive Control
  - Harmonic Compensation
  - Motor Control

Carrier Recovery



- General block diagram of frequency recovery from a modulated signal.
- When carrier has strong component in signal spectrum, PLL can lock.
- When carrier is missing from signal spectrum, PLL must be preceded by a nonlinear element.



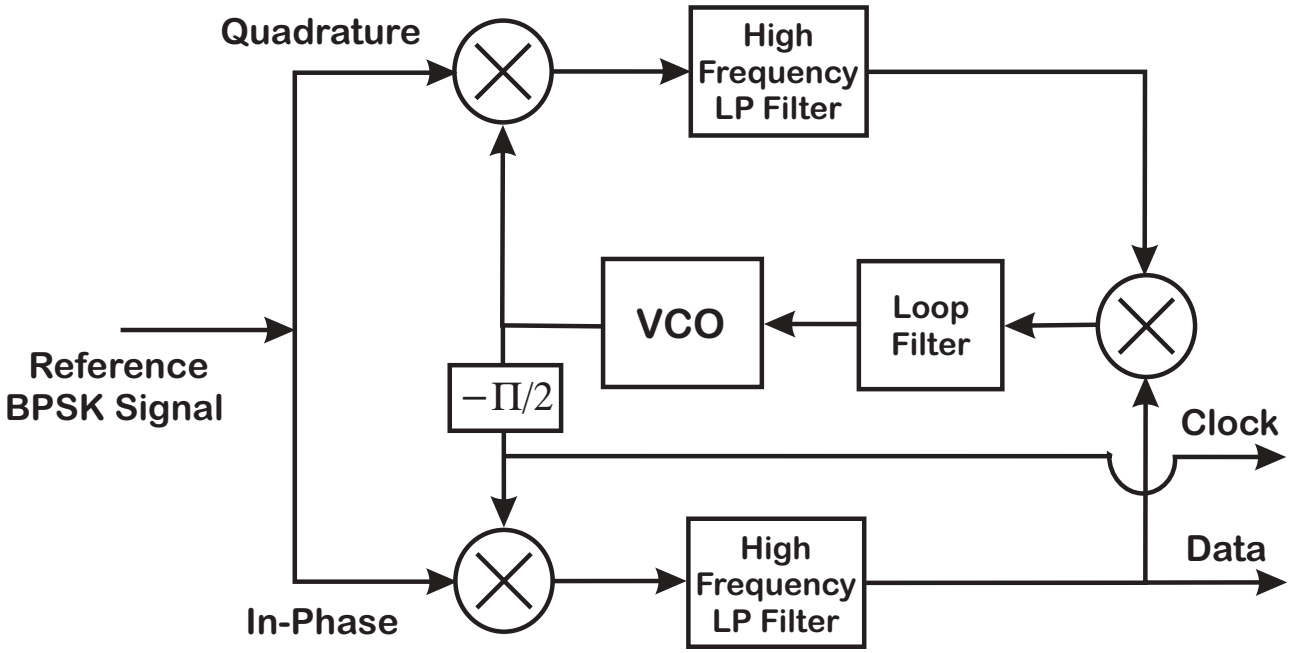
- Squaring loop to recover carrier from a BPSK modulated signal.
- Signal looks like

$$r(t) = m(t) \sin \omega_i t$$

  and $m(t)$ is ± 1.

- The spectrum of r has no component at ω_i (for equally probable $+1$ and -1 bits).
- Squaring loop locks to $2\omega_i$ and divide-by-2 circuit recovers ω_i.

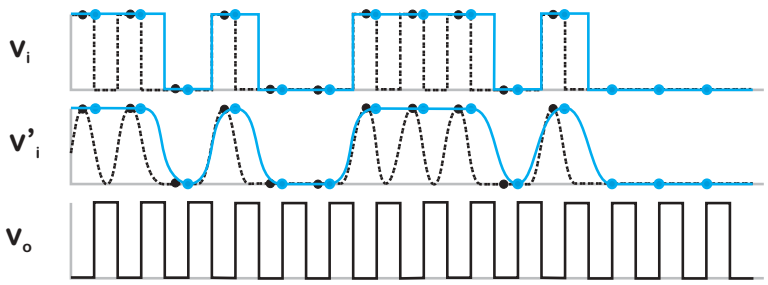
Costas Loop

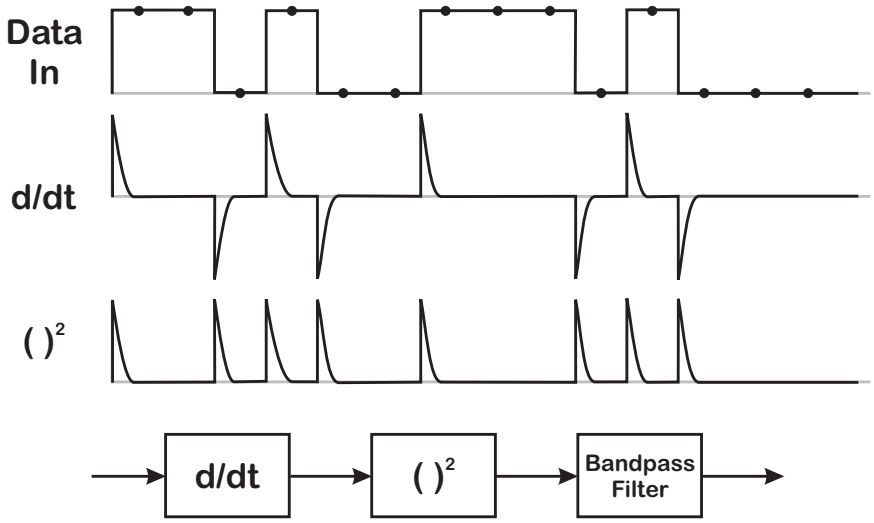


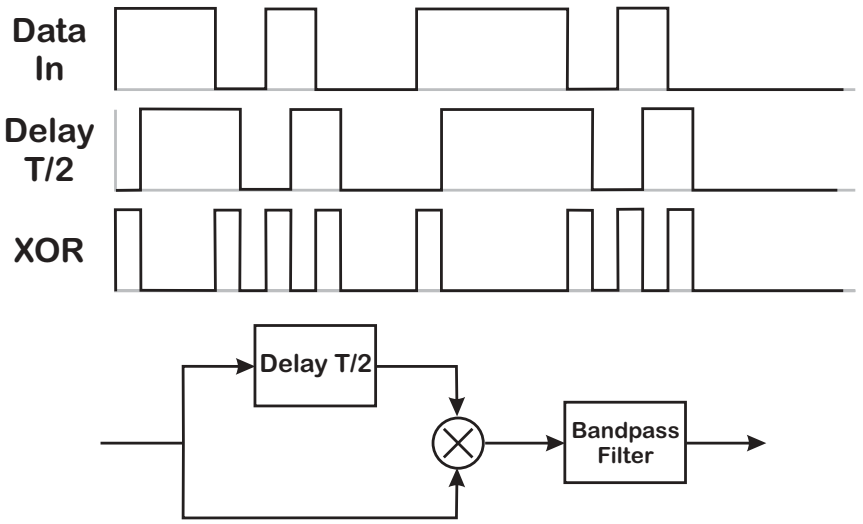
- A Costas loop can both recover the carrier and demodulate the data from such a signal.
- Intuitively, if there were no modulation, the upper arm is simply a PLL locks to a carrier.
- The effect of the lower arm of the loop is to lock to the modulation and cancel it out of the upper arm of the loop.
- Does the same thing as squaring loop, but down converts signal to baseband & does filtering there.
- Multiplier accomplishes same thing as squarer.

Clock/Data Recovery

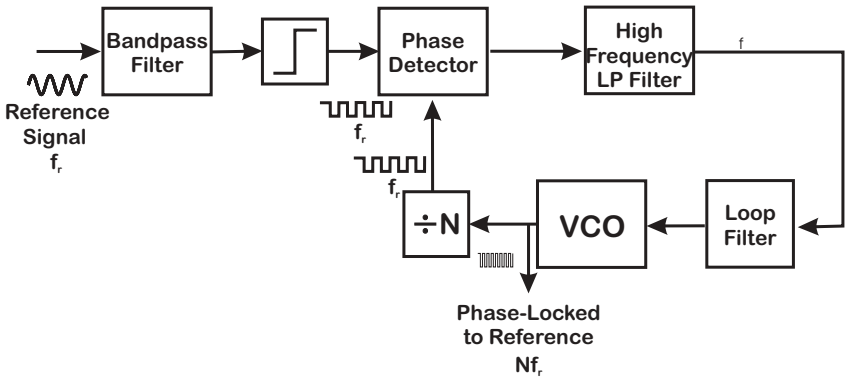
- RZ data (dark dashed) and NRZ data (solid light)
- On left, conversion from NRZ data to RZ data using analog circuits.
- On right, conversion from NRZ data to RZ data using digital circuits.
- Bang-Bang and Hogge detector recover clock directly from NRZ signal.



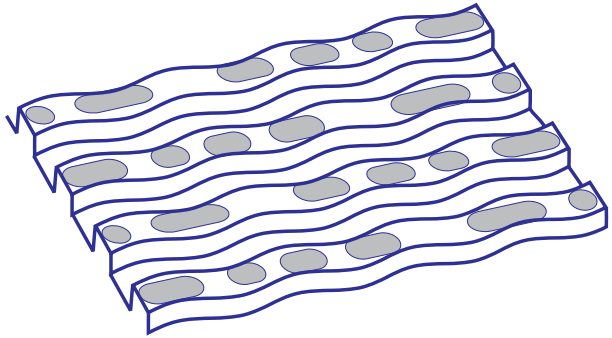


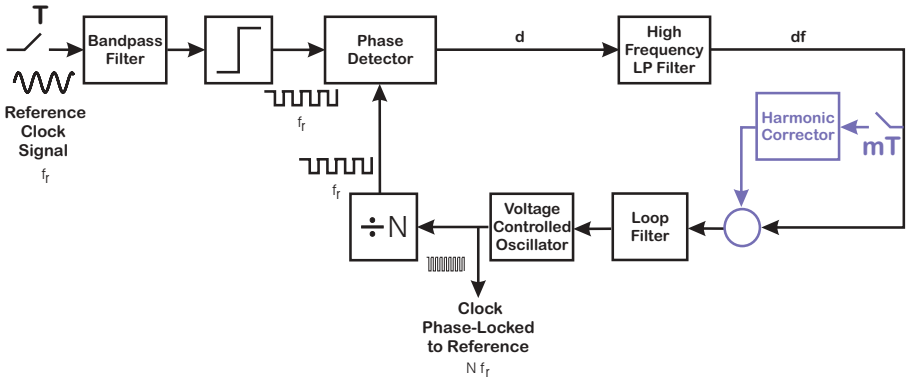


Frequency Synthesis



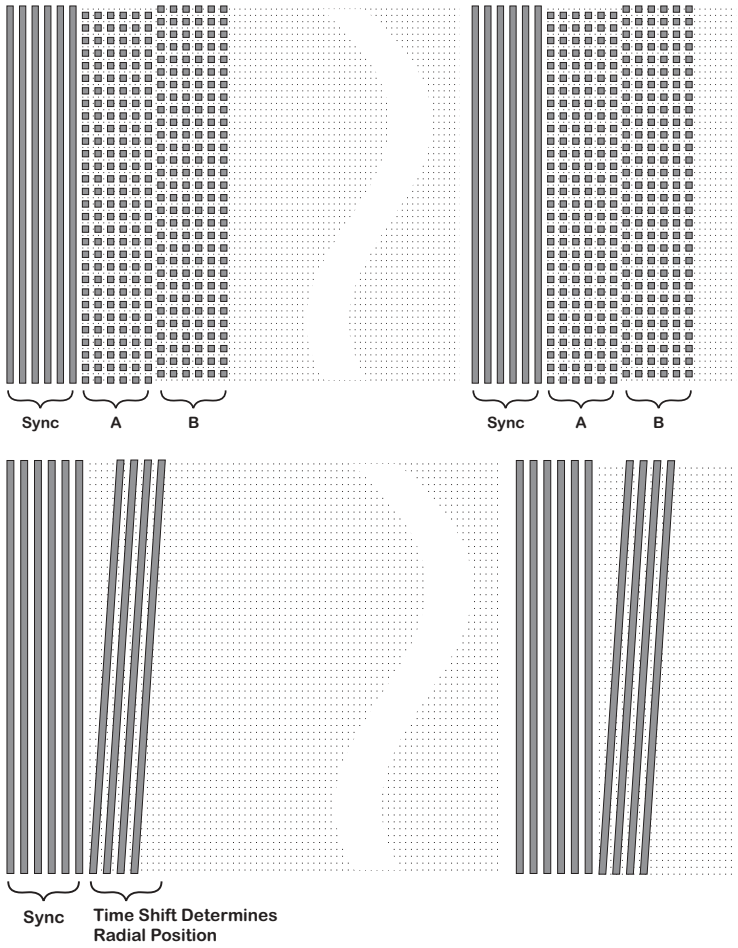
- Want to lock a clock with an input signal of a different frequency.
- Synthesize a clock frequency from a lower frequency input.
- Harmonic locking loop generates a clock at N times input frequency.
- Non-integer N is possible.
- Example from storage industry: DVD+RW format uses a high frequency wobble embedded in the groove walls to synthesize a write clock frequency.





- It is possible to remove harmonic phase modulation with a multi-rate harmonic corrector.

Disk Drive Control

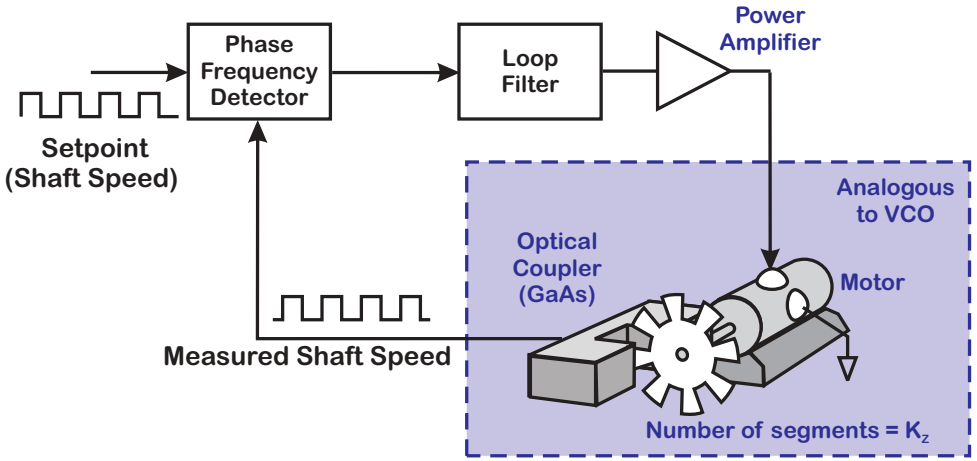


- Amplitude encoded position error signal (PES) in a hard disk. PLLs are used to time the acquisition of the readback signal.
- In phase encoding of position error the phase difference between the reference mark and the position mark gives a measure of the cross track position.

Harmonic Compensation

- Harmonic compensation when frequency is known is fairly well known.
- When frequency is not known, PLL techniques can be used. See Wu & Bodson in literature and later this session and Bodson & students in general.

Motor Control



- Optical coupler is a photodiode followed by a Schmitt Trigger $\Longrightarrow$ produces an oscillation proportional to the motor speed.
- Motor & optical coupler replace the VCO.
- Phase-frequency detector used $\Longrightarrow$ infinite pull in range and there are no missing samples.
- Motor model itself is second order:

$$G_m(s) = \frac{K_m K_z}{s(1+sT_m)},$$

K_m : motor torque constant, T_m : motor time constant, & K_z is the number of segments in the wheel.

- Motor control using PLL techniques replaces linear control with a speed setpoint as reference input and tachometer to measure rotational velocity.
- Tachometer has been replaced by an "optical tachometer" consisting of a segmented wheel attached to the rotor shaft and an optical coupler.
- Open loop response:

$$H_{OL}(s) = K_a K_d \left(\frac{1+s\tau_2}{s\tau_1}\right)\left(\frac{K_m K_z}{s(1+sT_m)}\right).$$

with K_a = PA gain, K_d = the PFD gain, & loop filter = integrator with minimum phase zero.

- During normal operation, the PFD in nonlinear regime as motor speed is ramped to different setpoints. Adkins, Marra & Walcott later this session improve steady state response by modifying the behavior of the PFD

Some Advanced Topics

- With all the available topologies and technologies, it should be clear that the choice of what to use is very application dependent.
- Digital techniques have the advantages that they are relatively immune to circuit drift and easy to integrate into small chip packages. However, they are not suitable for every application.
- For high noise input signals, the traditional mixer is still preferred as it makes the best use of information in the signal amplitude to reject noise. Classical digital PLLs are extremely useful in high speed digital communications systems.
- Some of the tradeoffs can be seen in high speed digital communications systems. As the standard for these systems reaches beyond 10 gigabits per second (Gbps), to 40 and 100 Gbps, the circuit technologies are hard pressed to produce the short pulses of phase detectors such as the linear Hogge detector. Thus, the nonlinear Alexander detector is often preferred. This is because the latter detector's components are easy to integrate and the detector itself has pulses that are no shorter than half a bit interval.
- At the extreme end, optical PLLs are being tested for clock/data recovery of 160 Gbps WDM optical communications.
- At the other end of the spectrum, as processing power goes up, it becomes more practical to sample the data and perform all the relevant operations in software Not only is this the ultimate in flexibility, but it can also be the lowest in cost.

Areas for Contribution: Where can control theory help?

- Nonlinear analysis. While many loop properties can be analyzed with linear models, this is not true for Bang-Bang loops, locking transients, and high frequency effects.
- Analyzing effects of noise injection from various components including phase detector and VCO.
- Improved analysis of intersample behavior of digital PLLs.
- Design tools to optimize designs of PLLs for both phase performance and signal performance.
- Some of these tools might also be useful in designing new phase detectors that are optimized for a particular type of loop.
- Design methods for high order PLLs. Loop shaping, etc. Often times PLL designers get forced by parasitic capacitances to deal with higher order loops. They have no rigorous analysis for this.
- VCO gain varies across units and over the frequency tuning range of the oscillator. We know how to handle this.
- Efficient simulation methods to allow for complete simulation of the system despite the two time scales would be very useful and could further be applied to software PLLs.

Useful References

- Andrew Viterbi's classic book (sadly out of print), Principles of Coherent Communication, has a wonderful first introduction to the analysis of a PLL. A. J. Viterbi, Principles of Coherent Communication. McGraw-Hill Series in Systems Science, New York, NY: McGraw-Hill, 1966.

- Floyd Gardner's famous little book, Phaselock Techniques, has been the classic first book for PLLs. It provides basic analysis and applications for PLLs. For many years, the first edition was the main book on the subject.

  F. M. Gardner, Phaselock Techniques. New York, NY: John Wiley & Sons, second ed., 1979. ISBN 0-471-04294-3.

- Another of the classic PLL text is Alain Blanchard's book, Phase-Locked Loops .

  A. Blanchard, Phase-Locked Loops. New York, NY: John Wiley & Sons, 1976.

- Dan Wolaver's book, Phase-Locked Loop Circuit Design provides excellent coverage of the different circuits used in PLLs, including many different phase detector models. Wolaver tends to focus on classical analog and classical digital PLLs.

  D. H. Wolaver, Phase-Locked Loop Circuit Design. Advanced Reference Series & Biophysics and Bioengineering Series, Englewood Cliffs, New Jersey 07632: Prentice Hall, 1991.

- Roland Best's book, Phase-Locked Loops: Design, Simulation, and Applications provides a more classical analysis of PLLs. It does an excellent job of describing the various classes of PLLs, including classical analog, classical digital, all digital, and software PLLs. Furthermore, a software disk is included. However, the treatment of actual circuits is far more cursory than Wolaver's book.

  R. E. Best, Phase-Locked Loops: Design, Simulation, and Applications. New York: McGraw-Hill, third ed., 1997.

- The IEEE Press has published two books containing papers on PLLs, both co-edited by William C. Lindsey. Phase-Locked Loops and Their Application, co-edited with Marvin K. Simon, contains many of the seminal papers on PLLs.

  W. C. Lindsey and M. K. Simon, eds., Phase-Locked Loops and Their Application. IEEE PRESS Selected Reprint Series, New York, NY: IEEE Press, 1978.

  Phase-Locked Loops, co-edited with Chak M. Chie, has a larger emphasis on digital loops.

  W. C. Lindsey and C. M. Chie, eds., Phase-Locked Loops. IEEE PRESS Selected Reprint Series, New York, NY: IEEE Press, 1986.

  A third book from the IEEE, edited by Behzad Razavi on Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design goes into much more depth on issues of integration of PLLs and CDR circuits into silicon. The collection starts with an excellent tutorial.

  B. Razavi, ed., Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design. IEEE PRESS Selected Reprint Series, New York, NY: IEEE Press, 1996.

- Hsieh and Hung have a nice tutorial on PLLs that not only includes the basic theory, but also some applications, particularly to motor control.

  G.-C. Hsieh and J. C. Hung, "Phase-Locked Loop techniques — A survey," IEEE Transactions on Industrial Electronics, vol. 43, pp. 609–615, December 1996.

- Paul Brennan's book, Phase-Locked Loops: Principles and Practice is a brief book with a practical bent. It gives an excellent explanation of phase-frequency detectors and charge pumps.

  P. V. Brennan, Phase-Locked Loops: Principles and Practice. New York: McGraw Hill, 1996.

- Donald Stephens has a book with an interesting history section in the front as well as a method of approaching analysis of digital PLLs that is closer to a typical sampled data approach than most books. This second edition of the book includes information on optical PLLs.

Phase-Locked Loops for Wireless Communications: Digital, Analog and Optical Implementation. Understanding Science and Technology, Boston/Dordrecht/London: Kluwer Academic Press, second ed., 2002.

- Someshwar Gupta's survey paper provides a history of analog PLLs to that point.

  S. C. Gupta, "Phase-locked loops," Proceedings of the IEEE, vol. 63, pp. 291–306, February 1975.

- William C. Lindsey and Chak M. Chie have a survey paper that outlines the history of digital PLLs up until 1981.

  W. C. Lindsey and C. M. Chie, "A survey of digital phase-locked loops," Proceedings of the IEEE, vol. 69, pp. 410–431, April 1981.

Acknowledgments

The understanding of PLL circuit components presented here has been greatly enhanced by discussions with

- Rick Karlquist, Rick Walker, and Len Cutler of Agilent Laboratories
- Dr. Salam Marougi of Agilent Technologies' Electronic Products and Solution Group.

The control systems interpretation of various loop components improved dramatically after discussions with Prof. Gene Franklin of Stanford University.

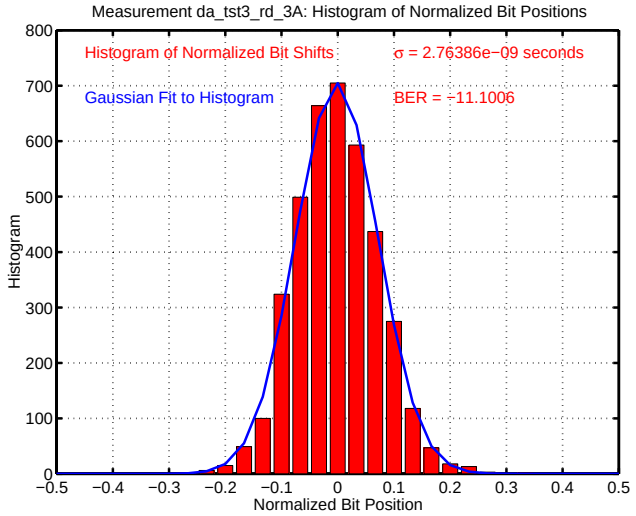
This talk came from a special session at the 2002 ACC. The session would not have happened without the rapid generation of papers by the other session members:

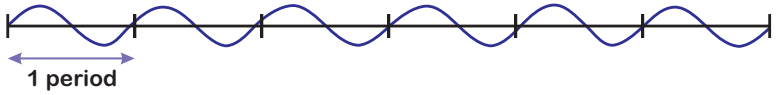
- Prof. N. Eva Wu of SUNY Binghamton
- Chris Adkins and Mike Marra (both of Lexmark) and Dr. Bruce Walcott from the University of Kentucky
- Biqing Wu and Prof. Marc Bodson of the University of Utah

Dan Witmer of Openwave who walked into my office at Ford Aerospace 18 years ago and asked, "How would you analyze a nonlinear phase-locked loop?"

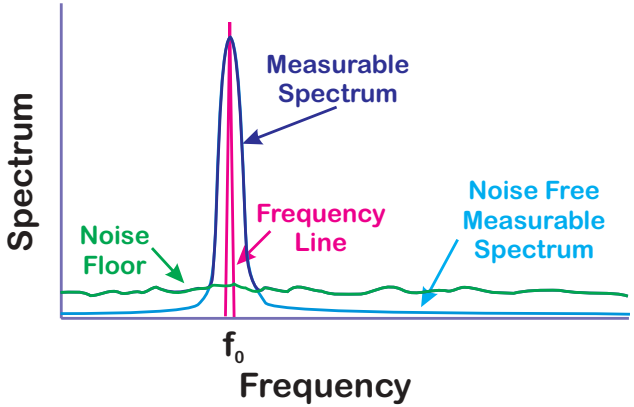
Jitter Happens

- Jitter is a timing variation with respect to some reference timing.
- Jitter is to timing as noise is to level
  $\Longrightarrow$ essentially jitter is timing noise.
- There are many different ways to precisely define and measure jitter.
- Jitter is usually measured relative to a clock period or a bit period.
- Jitter can also be measured in time units.





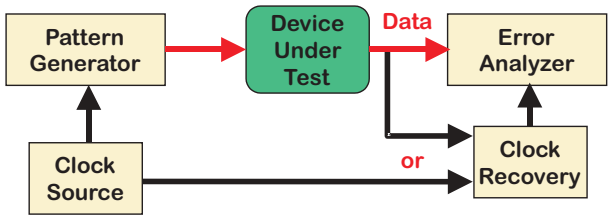
- In the frequency domain, jitter becomes phase noise.
- Jitter is measured relative to some carrier signal, which is equivalent to measurement relative to a bit interval.

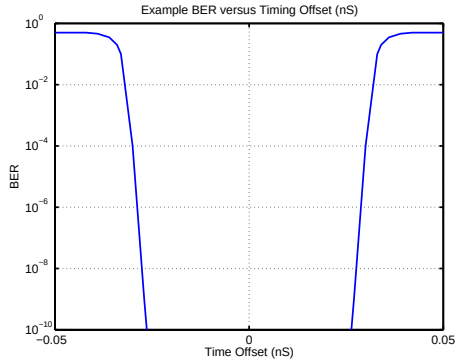


Jitter Measurements

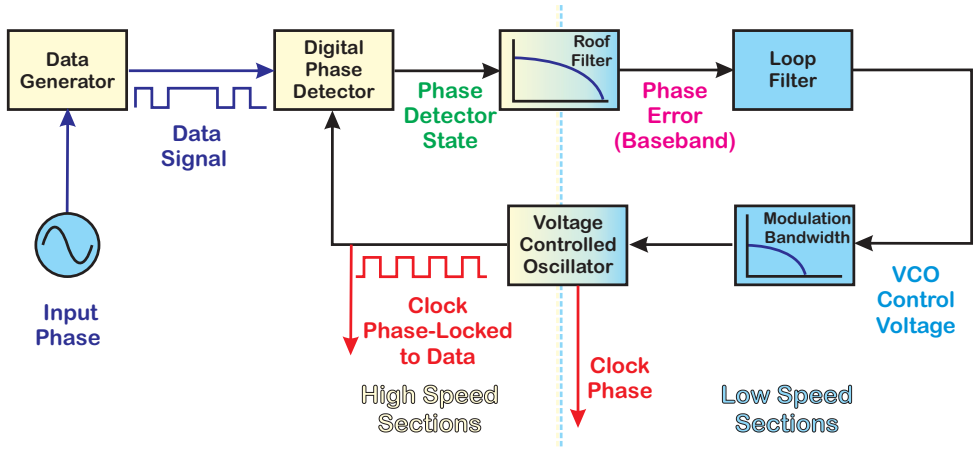
For two signals, A and B, jitter is measured in several different ways (A versus A, A versus B, B versus B):

- **Time Domain**
  - Measure timing variation of A, B.
  - Normalize by bit/clock period.
  - Comupute histogram
  - Fit curve
  - Estimate BER
- **Frequency Domain**
  - Spectrum analysis
  - Look at deviation from carrier/clock
  - Normalized as $\frac{df}{f}$
  - Limited by resolution bandwidth of measurement
  - Need to know the properties of clock used for spectrum analysis.
- **Bit Error Rate Tester (BERT)**
  - Measure BER versus timing variation across a bit interval.
  - Compute bathtub curve/eye map.
  - Look at eye opening at specified BER level.
  - Computes total BER.





Time Domain Jitter Measurement



- Consider the clock recovery loop above.
- We can measure jitter in:
  - recovered clock versus itself
  - data signal versus clock

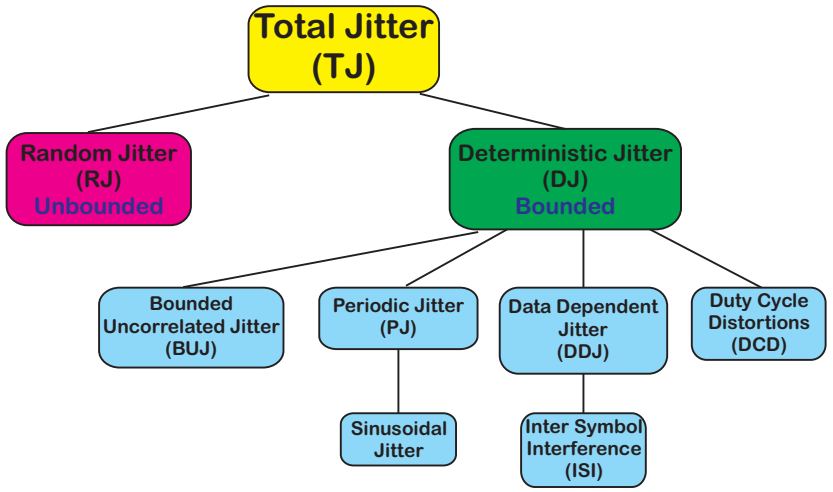
- leading edge to trailing edge
- leading edge to leading edge
- trailing edge to trailing edge
- peak to peak or RMS
- Total Jitter, Random Jitter, Deterministic Jitter

...

- If clock is not transmitted with data, need to recover clock.
- Jitter measurement is no better than recovered clock.
- With so many ways of measuring/defining jitter, it's no wonder you can't find a cohesive view of the field.

Some Thoughts on Jitter and PLLs

- At some point, each method requires a clock. Jitter in this clock affects the measurement.
- If clock is not transmitted with data, need to recover clock.
- Jitter measurement is no better than recovered clock.



- Jitter is broken down into random and deterministic jitter.
- Random jitter is assumed driven by Gaussian noise. Deterministic jitter is broken down further.
- With so many ways of defining/measuring jitter, it's no wonder you can't find a cohesive view of the field.
- Yet understanding jitter is crucial as clocks and signals get faster, thereby lowering bit intervals in digital systems.
- A systems view of this should help a lot.