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Turning the Tracking Problem Sideways: Servo Tricks for DVD+RW Clock Generation

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Abstract

This work describes a write clock generation scheme for rewritable DVD which eliminates a major issue for drop-in compatibility with DVD-ROMs. In order to do this, several tricks from servo systems are employed to improve the write clock. Fundamentally, the method used is to co-locate a high frequency clock reference next to the data using a wobble groove. A variety of methods are considered to compensate for readback signal distortion caused by different laser powers during reading, erasing and writing of data. Finally, harmonic compensation can be added to the clock to eliminate the effects of eccentricity and spindle variations. The result is the ability to do bit accurate edits on rewritable DVD media.

1 Motivation

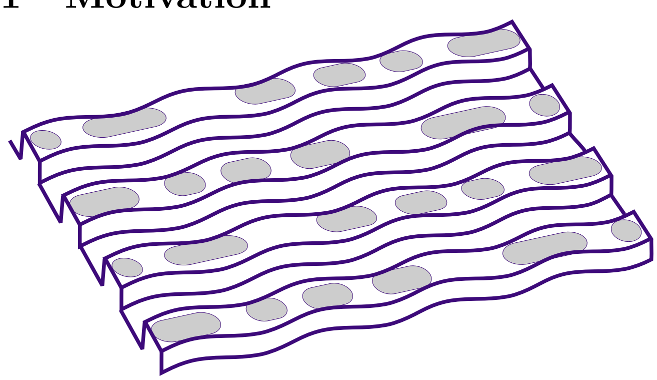

Figure 1: A perspective schematic of high frequency wobbles.

This paper presents a controls oriented perspective[1] on a new method of write clock generation on rewritable DVD drives that eliminates many of the problems associated with reading rewritable disks in DVD-ROM drives. It is believed that such a format will provide tremendous benefits to the end user, making it possible to edit content on a rewritable DVD disk and then play that same disk in a conventional DVD-ROM player. From a large set of potential problems, it appears that the real issues can be reduced to two:

- smaller changes in reflectivity for written bits on phase-change media as compared to stamped media and
- a much tighter clocking requirement caused by the need to eliminate edit gaps.

Of these, the first is an issue for roughly half of the commercial DVD players in the world today. This issue can be overcome in the remainder rather trivially with a simple circuit change in the automatic gain control (AGC) of the reader. It is the latter issue which is a problem. As shown in Figure 2, DVD-ROM disks have no edit gaps or physical sector marks. This is in contrast to conventional rewritable formats which need these gaps to accommodate imprecision in the write clock which would otherwise cause data loss at the end of data fields [2, 3, 4, 5, 6].

2 High Frequency Wobble Clock

In order to eliminate these edit gaps a new clocking scheme was devised that uses high spatial frequency groove edge oscillations (wobbles) to generate clock signals. This has the advantage that it co-locates clock reference with data, yielding a high fidelity, high frequency clock reference. Using this, one can lock a narrow band phase-locked loop (PLL) to the oscillation frequency to generate the write clock. Addressing information can be encoded into the wobble itself using a variety of methods to eliminate the need for physical sector marks.

Having a continuous clock co-located with the data is more precise and robust than intermittent clocks. The PLL can average over many clock cycles to ignore defects more easily. Furthermore, spindle runout, disk eccentricity and thermal variations have far less effect on the write clock. This means that there is virtually no drift between

[1]For an optical recording centered perspective see [1].

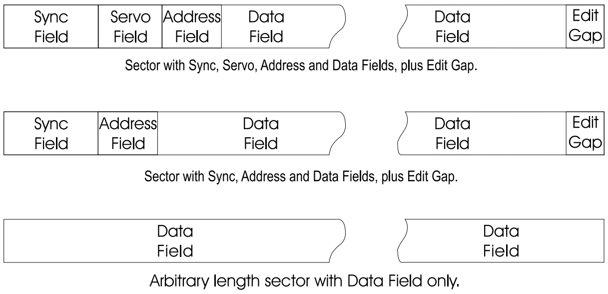

Figure 2: Optical disk formats on rewritable and ROM media. The top diagram represents sector formats on drives where synchronization, servo, and address fields as well as an edit gap are time multiplexed down the track with the data. This is the current norm in both sampled servo magnetic and optical disk drives. The middle diagram represents sector formats on drives which do not obtain their servo information from the sector header, but still time multiplex the remaining fields with the data. This was common in dedicated servo magnetic drives, which have fallen out of favor, and is the norm in optical drives where the grooves or pits provide a continuous pattern for the tracking servo. The top two formats are the prevalent methods used in rewritable magnetic and optical media. The bottom digram represents a typical format for ROM media. Because the media is mastered once at the factory, no physical sector marks are needed. Instead, logical synchronization and address fields are included within the data.

clock samples, allowing for the elimination of edit gaps. By encoding address information in the wobble itself, the embossed sector information is "off to the side" of the data. This clears the way to make the data sector continuous, as in the DVD-ROM format [7].

3 Implementation Choices

While there are many possibilities for implementing such a scheme, the choice of the specific physical encoding method depends upon the available spatial frequencies, the available signal detection methods, and a desire to avoiding interference between clock and data/servo signals.

Once it was decided that the highest probability of success for a product would be in a system with a near industry standard set of optics (0.6-0.65 NA lens, 635-650 nm laser), the possibility of putting the clock frequency above the data frequencies was eliminated. Putting the clock frequency below the data frequencies would have resulted in a write clock with too much jitter. The solution is a high frequency wobble groove – an in-phase oscillation of the groove walls – as the method for encoding the reference clock. This has the advantage that it is nominally invisible to data detection in the central aperture mode, but yet easily detectable in the radial push pull servo signal outside of servo bandwidth. This allows the wobble signal to be encoded within the range of data frequencies with little interference between the two signals.

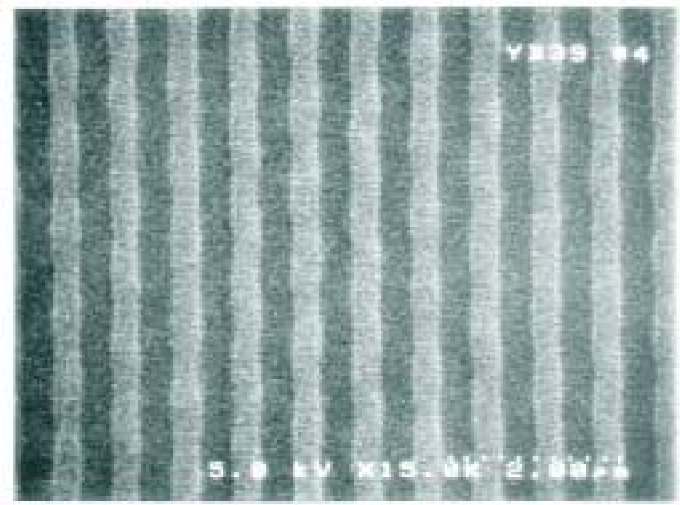

Figure 3: SEM Image of 4.7 GB, 30 nm Peak to Peak Wobble Disk

4 PLL Issues

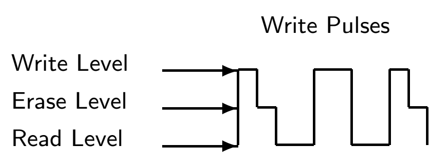

Figure 5: Write pulse diagram.

The signal read back from the high frequency wobble becomes the reference clock signal for the system. The write clock is generated by using a harmonic locking PLL [8, 9] as shown in Figure 4 to boost the reference clock frequency to that of a write clock. The limiter preceding the loop makes it insensitive to amplitude changes resulting from laser power changes when switching between reading and writing.

It turns out that various drive related issues can be resolved by making adjustments to the PLL that are typical of real world control systems. This section will discuss several of those issues as well as potential improvements.

A schematic diagram of the optical drive with a PLL for write clock generation is shown in Figure 4. Two potential problems arise from this configuration which can

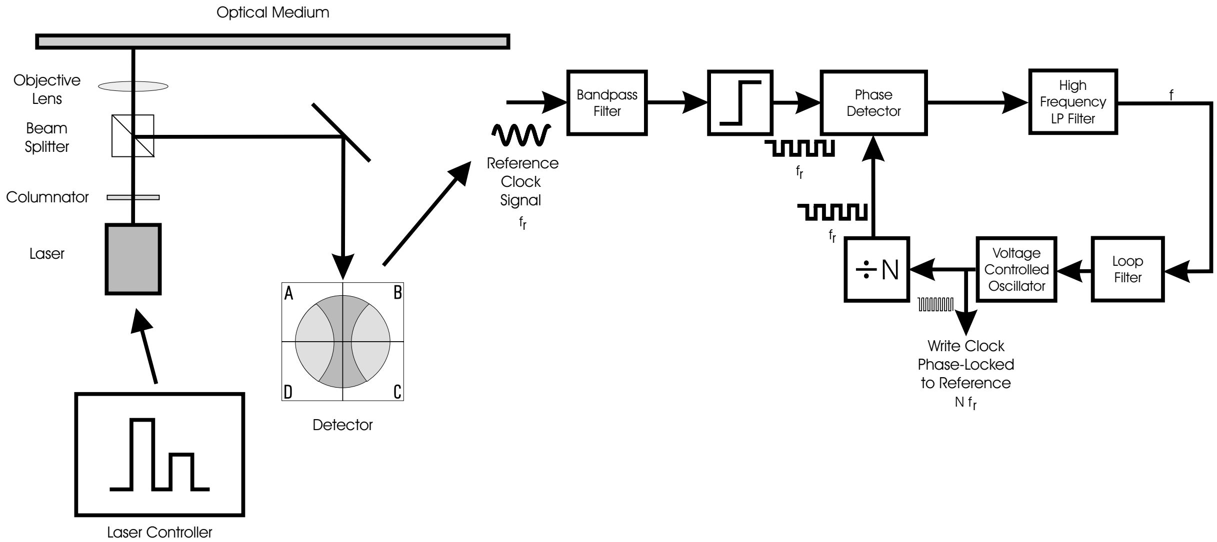

Figure 4: Rewritable optical disk drive system with a Harmonic Locking PLL to generate the write clock.

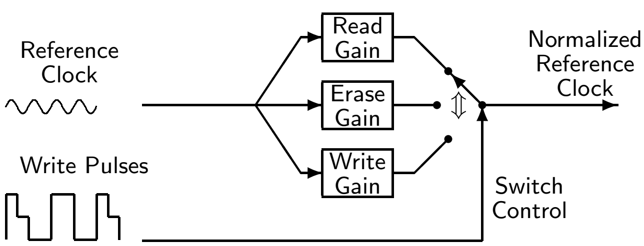

Figure 6: A "gain-scheduling" method of high speed signal normalization.

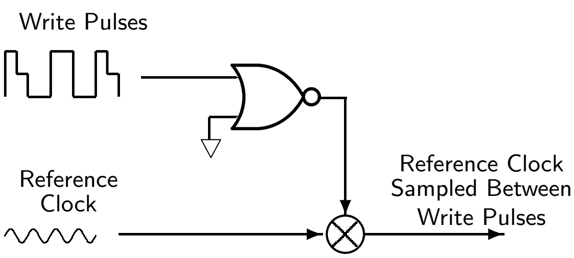

Figure 7: Sampling between write pulses.

be addressed in the PLL.

The first is that sudden changes in amplitude of the readback signal can cause phase errors because the loop is unable to distinguish (at high speed) the difference between an amplitude difference and a phase difference. Furthermore, in a classical mixing loop, these amplitude changes result in a change in the open-loop gain of the PLL. In the case of a phase change rewritable optical disk drive, the transitions in laser power from read to write to erase levels, as shown in Figure 5, cause these changes in readback signal amplitude. These sudden changes in amplitude are far too fast for an automatic gain control circuit (AGC) or a normalizing circuit which is typically found in an optical disk drive.

The second is that spindle eccentricity and offsets in mounting of the removable media can affect the accuracy of the clock. Even if a harmonic corrector is used in the tracking loop, the act of following a noncircular path will result in timing differences of the reference signal. The challenge is to reduce these effects while maintaining a low bandwidth PLL (for noise immunity).

4.1 Laser Power Issues

There are 3 distinct possibilities of addressing such problems. The first is to use a limiter with very low phase dispersion to reduce the amplitude of the signal to simply an indication of the zero crossing time. This is a common method of implementing a phase locked loop and generates a triangular phase characteristic [8] which is convenient for linear analysis.

The potential disadvantage of such a loop is that it may have less noise immunity than a classical mixing loop (see Wolaver [8], page 54, and Crawford [9], page 81). For improved noise rejection, there are advantages to using a classical mixing loop which makes full use of the amplitude information. The key question is how to adjust for the amplitude changes due to the writing process.

Two possible solutions are inspired by the fact that the drive itself has knowledge of the write signal that it is sending to the laser and thus it has knowledge of the amplitude changes in the returned reference clock signal. The drive can use this knowledge in one of two ways: to do a feedforward gain adjustment reminiscent of gain-scheduling (Figure 6) or to sample the reference clock signal between write/erase pulses (Figure 7). The result is sent to the bandpass filter in front of the PLL.

In either case, the adjustments cause the loop to not see any of the amplitude changes and thus maintain a constant gain. Thus, these adjustments allow the use of a classical mixing loop with its improved noise immunity but at the expense of greater complexity in the case of the gain-scheduling case (Figure 6) or some loss of signal in the sampling case (Figure 7). In the case of the experiments done at HP Labs, it turned out that the solution that used the limiter had sufficiently low write clock jitter so that the latter two solutions were not needed.

4.2 Harmonic Cancellation

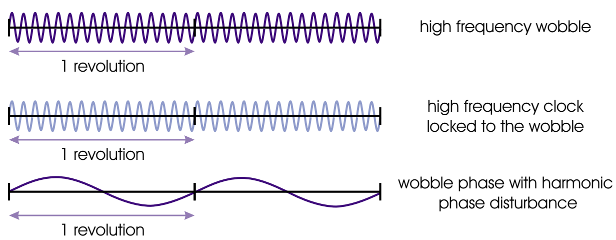

Figure 8: Harmonic Phase Errors in a PLL

As with most servo loops, there is a desire to minimize the bandwidth of the write clock PLL to minimize the amount of noise passed to the PLL output. In this case noise passed through the system directly affects the write clock and thus the final data jitter. However, offsets caused by eccentricity can also appear to the data channel as jitter and thus should be minimized. The solution then is to use the same type of harmonic compensation on the PLL as is typically done on tracking loops [10, 11, 12].

Note that the harmonic corrector can have many forms including the classic repetitive controller and the adaptive feedforward controller [12]. An example of such a loop is the PLL shown in Figure 9. Note that this loop can also be made a digital PLL by sampling the reference clock with a period of T as shown in Figure 10. This structure allows for the possibility of multirate control, which is desirable because even though the wobble signal is in the range of MHz frequencies, the spindle induced oscillations are in the tens or hundreds of Hz. An example simulation is shown in Figure 11. The simulation wobble frequency and time scales had to be adjusted away from the actual wobble frequency, as simulating multiple spindle revolutions worth of PLL data with the true wobble frequency would have required a prohibitive amount of computer memory. Nevertheless, the simulations provide useful understanding of the behavior of the true hardware PLL. This simulation uses an adaptive feedforward compensator to implement the harmonic corrector. The loop itself uses the multirate structure of Figure 10, but uses a classical mixing loop for improved numerical results.

5 Results

It turns out that the limiter/phase-detector implementation of the harmonic locking PLL provided sufficient amplitude immunity for the experiments. The resulting system is one that makes bit accurate editing a reality. A typical example of this is shown in Figure 12, where a 6T pattern (6T mark, 6T space) is spliced into a 4T-8T pattern with negligible phase error.

Results such as this have been reliably repeated for a variety of edits and a variety of disturbance conditions. They indicate that the scheme has good robustness to radial and tangential tilt, offtrack, defocus, and modulation of the wobble for addressing [1]. By making linkless editing a reality, this project has provided a key feature of the DVD+RW 4.7 GB optical disk format.

6 Acknowledgements

While this paper has centered on the controls aspect of high frequency wobbles work at HP Labs, the project itself took the effort of many engineers to make it a reality. Those people include Daniel Abramovitch, David Towner, Craig Perlov, Josh Hogan, Michael Fischer, Carol Wilson, Ilkan Çokgör, and Carl Taussig.

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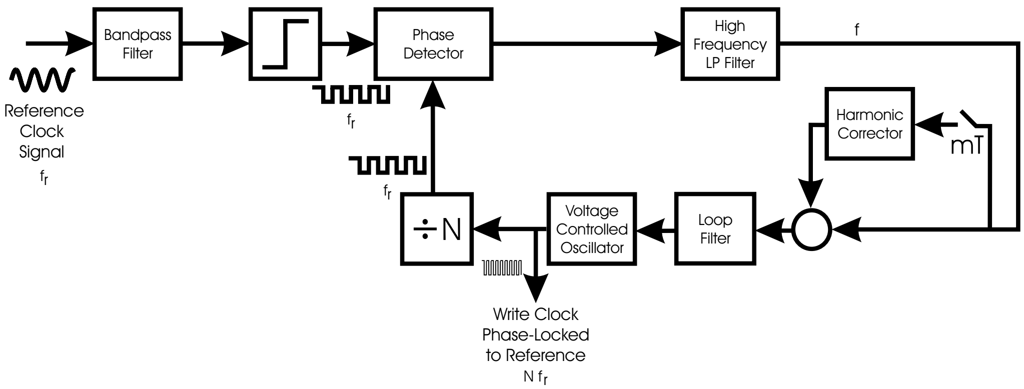

Figure 9: A Harmonic Locking PLL which uses a phase detector. This has a Harmonic Corrector tapping off of filtered phase error output, Ψ_f. This configuration that is implementable in hardware.

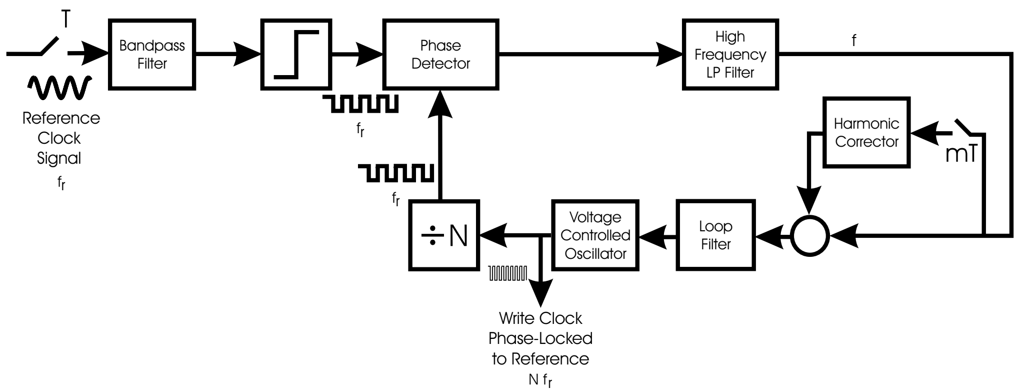

Figure 10: A Sampled Harmonic Locking PLL which uses a phase detector. This has a Multirate Harmonic Corrector tapping off of filtered phase error output, Ψ_f. This configuration that is implementable in hardware.

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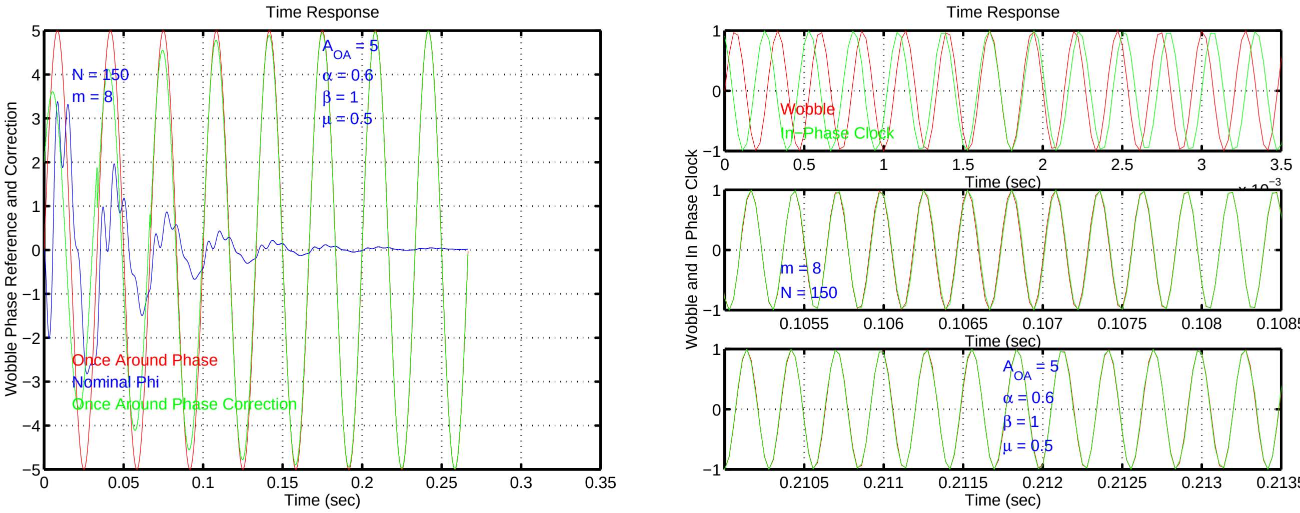

Figure 11: Simulation Results: Multi-rate once around correction with disturbance amplitude = 5 radians. This plot shows phase (left plot) and clock (right plot) results when the harmonic corrector is subsampled at $\frac{1}{8}$ times the sample rate of the PLL simulation. Specific parameters: $N = 150 =$ wobble samples/revolution, $m = 8 =$ subsample factor for harmonic corrector, $\alpha = 0.6 =$ initial phase accuracy of corrector ($1 =$ correct), $\beta = 1 =$ initial amplitude accuracy of corrector ($1 =$ correct), $\mu = 0.5 =$ adaptation rate for adaptive feedforward compensation.

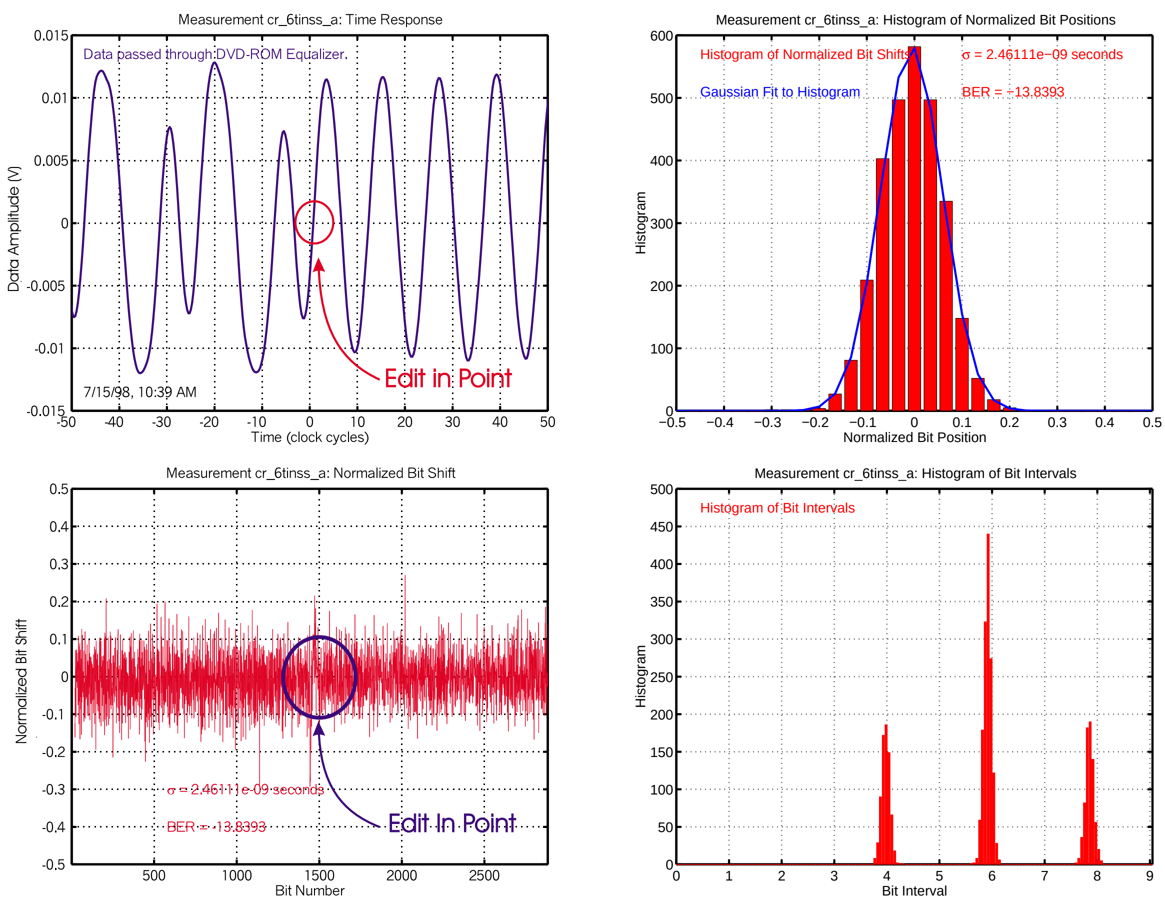

Figure 12: A 6T pattern spliced into a 4T-8T pattern. The upper left plot represents the time response at the edit-in point. The lower left represents the phase error for a data clock generated from the data. (Note the absence of any phase jumps.) The upper right plot is a histogram of the normalized bit positions from which a bit error rate can be computed. The lower right is a set of histograms of the bit intervals. The absence of any 5T or 7T bits is an indication that no bit errors have occurred.