

## Turning the Tracking Problem Sideways: Servo Tricks for DVD+RW Clock Generation

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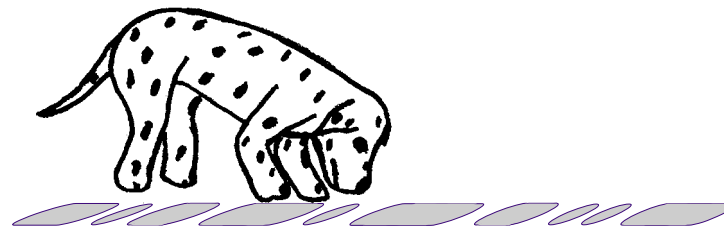
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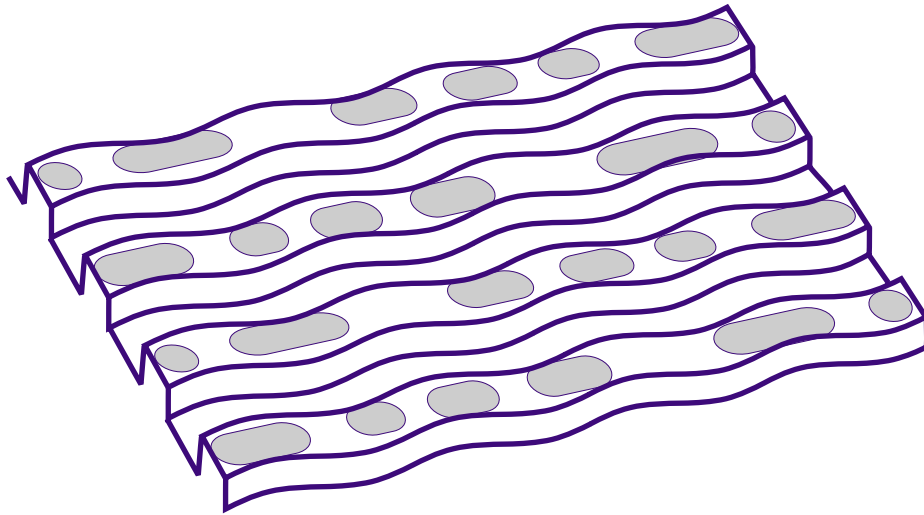


Slides and digest available at: [http://www.labs.agilent.com/personal/Danny\\_Abramovitch/pubs/](http://www.labs.agilent.com/personal/Danny_Abramovitch/pubs/)

## Talk Outline

- Problem statement: clocking rewritable DVD
- Structure & choices for clock structure
- Write clock generation loop
- Linkless editing results for 9T wobbles
- Adjustment due to format negotiated 31T wobbles
  - adjustments to PLL for laser power
  - harmonic correcting PLLs
  - harmonic correcting PLL results
- Write strategy adjustments
- Jitter results
- Crosstalk results (wobble  $\longleftrightarrow$  data)
- Conclusions

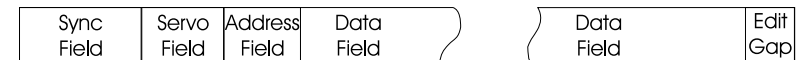
## Problem statement: clocking rewritable DVD



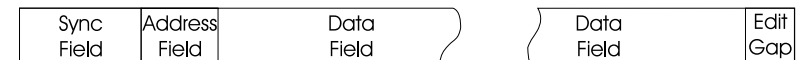
- We want a rewritable 4.7 GB DVD whose output is DVD-ROM compatible.
- Technical problems can be summarized as:
  - writing smaller spots
  - harder tracking requirements
  - reflectivity issues
  - much harder clocking requirements

## Requirements for a Clocking Scheme

- DVD-ROM disks have no edit gaps or physical sector marks.
- Writable formats have edit gaps and physical sector marks.
- We must eliminate these.
- A high frequency clock with addressing embedded in the groove walls can solve these problems.



Sector with Sync, Servo, Address and Data Fields, plus Edit Gap.

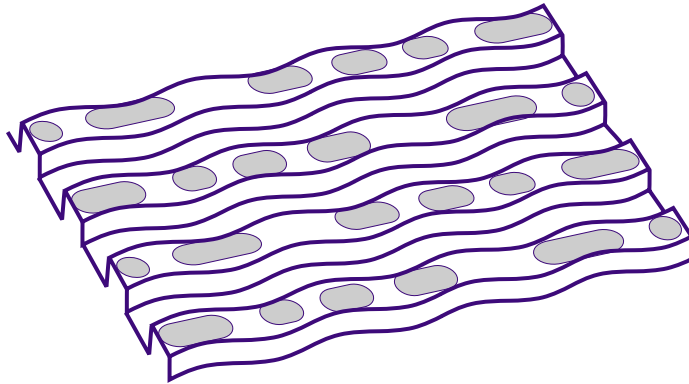


Sector with Sync, Address and Data Fields, plus Edit Gap.

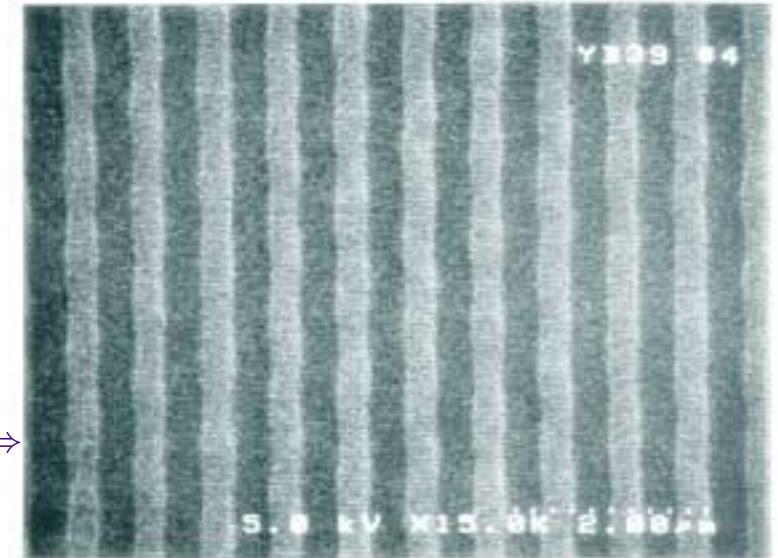


Arbitrary length sector with Data Field only.

## A High Frequency Clock Reference Structure

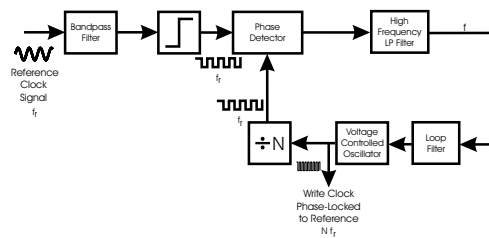


- Wobble groove walls at high frequency as a clock source.
  - Co-locates clock reference with data.  
⇒ high fidelity, high freq. clock reference
  - Lock narrow band PLL to oscillation frequency.
  - Encode address info. in the wobble.
- This results in a write clock that is:
    - very accurate ⇒ jitter < 300 pS < 1 % of a data clock bit ( $T \approx 38$  nS) (for 9T wobbles)
    - orthogonal to the data ⇒ data and wobble detected in different ways
    - very robust to:
      - \* offtrack and defocus
      - \* radial and tangential tilt
      - \* defects and missing wobbles
      - \* temperature and spindle variations
  - Continuous data sector, as in DVD-ROM.
  - SEM photo of 30 nm Peak to Peak Wobbles ⇒

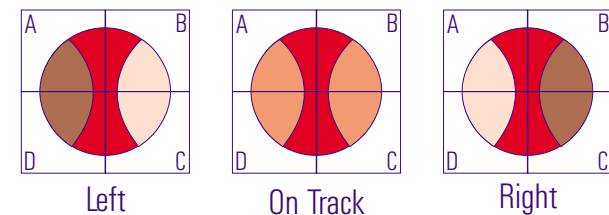
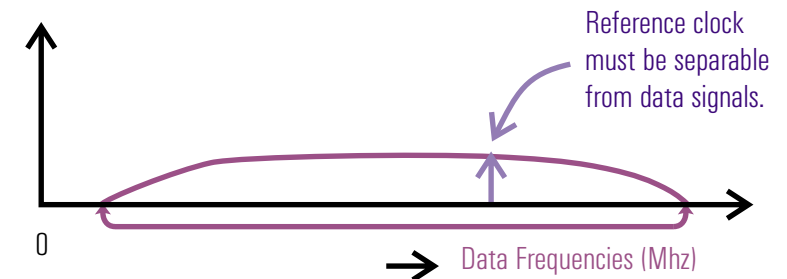
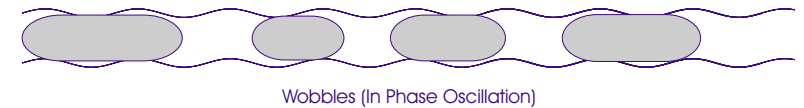
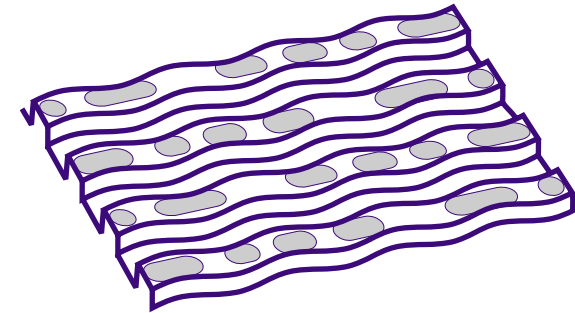


## Implementation Choices Guided by Industry Direction

- Same optics as DVD-ROM
  - ⇒ Clock must be buried in the data frequencies
  - ⇒ Use wobble grooves
- Seen in servo signal, suppressed in data signal
- PLL generates write clock

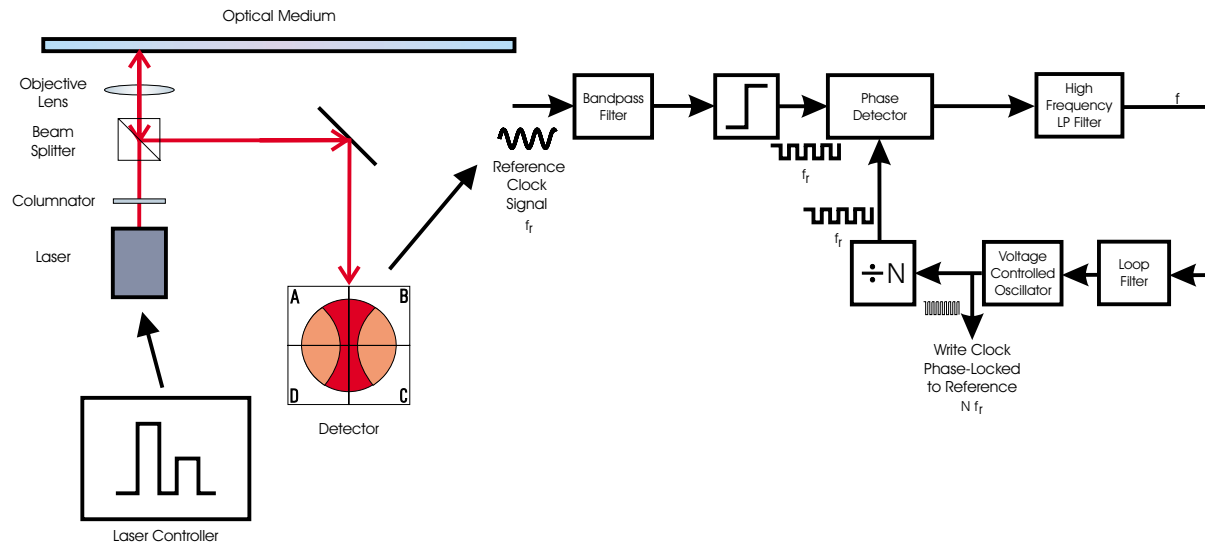


- Splice accuracy  $< 0.2T$  (data clock bit) (9T Wobbles)
  - ⇒ Closest known claim is 7T
- Media partner can manufacture the disks.
- HPL has prototyped the electronics.
- Several available methods for addressing.



Wobble Detected in the Un-normalized Radial Push Pull Tracking Signal

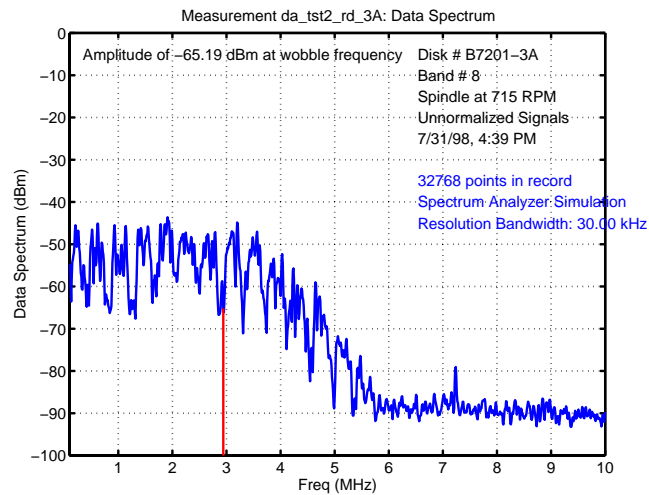
## Rewritable optical disk drive system with a Harmonic Locking PLL to generate the write clock



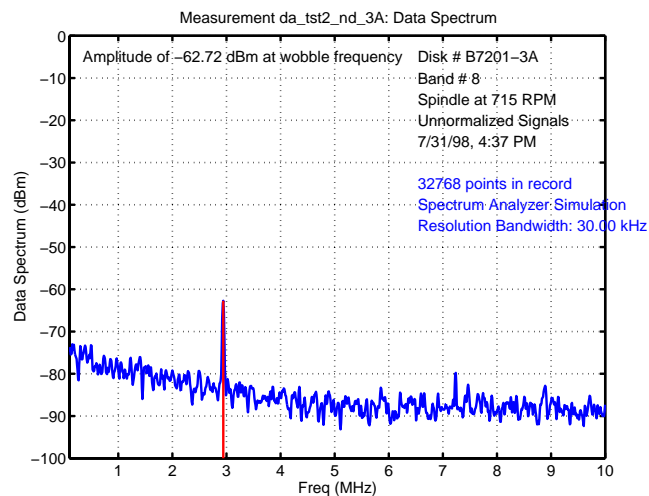
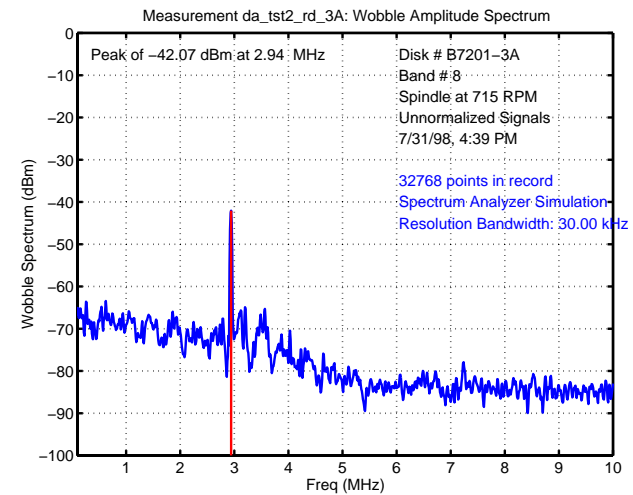
Clocking requirement is stringent however:

- Data and wobble share common frequency range.
- Changing laser levels (read/write/erase) mean dramatically different power levels at photodetector
- Rotating disk has eccentricity which shows up in clocking loop.

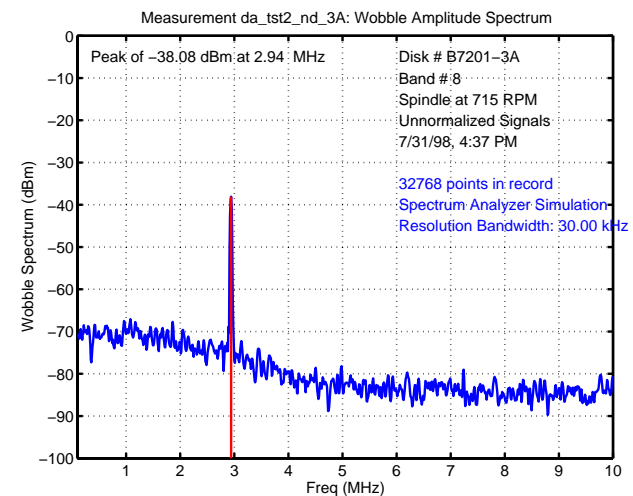
## Crosstalk Between Data and Wobbles is Small



Random  
Data  
on  
Track



No  
Data  
on  
Track

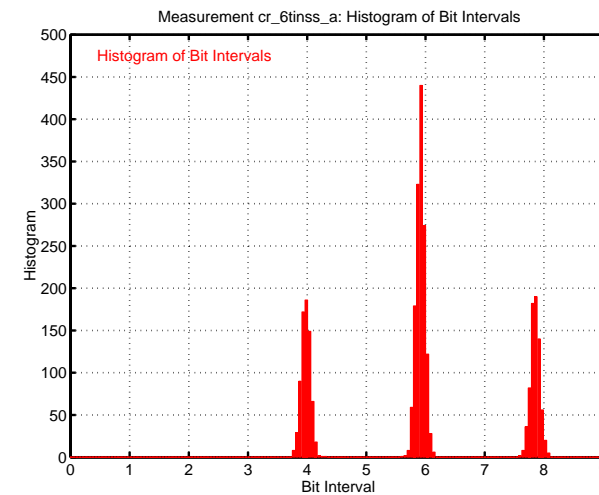
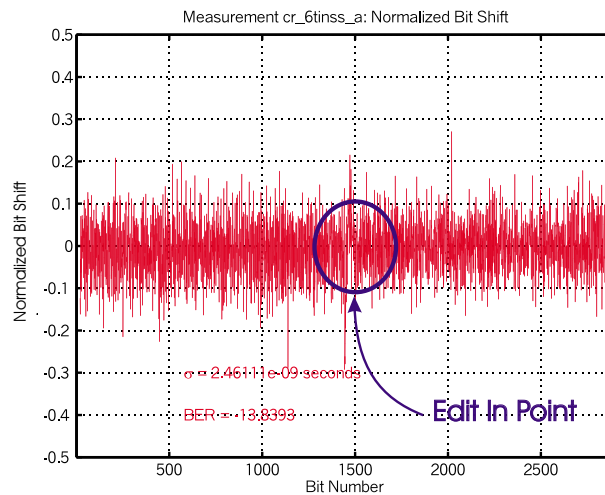
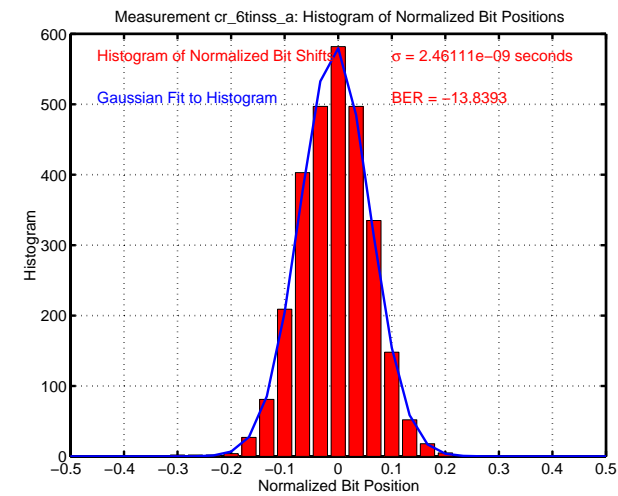
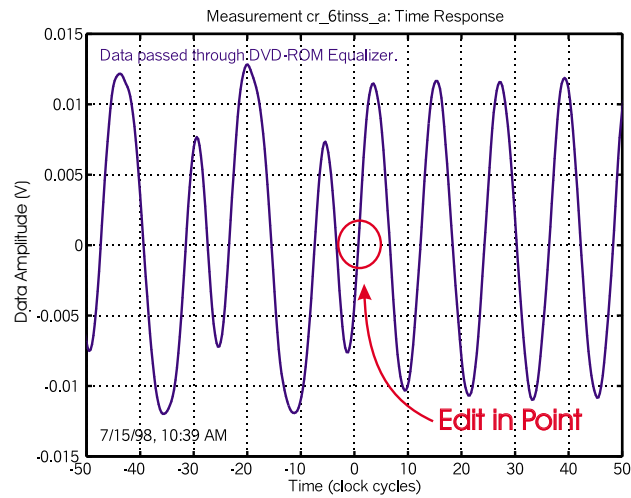


Data Channel Spectrum

Wobble Channel Spectrum

- no significant effect of one on the other

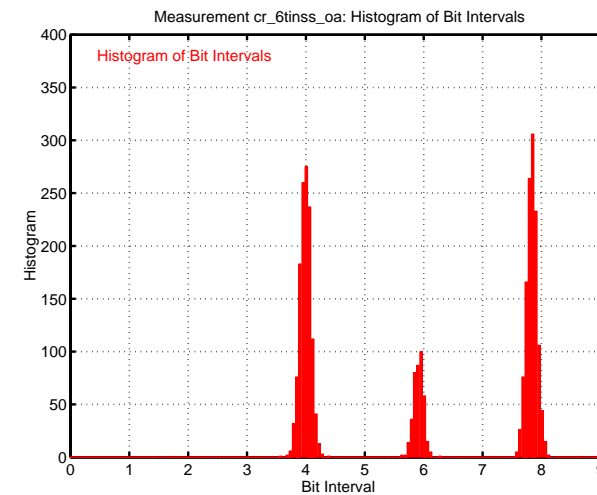
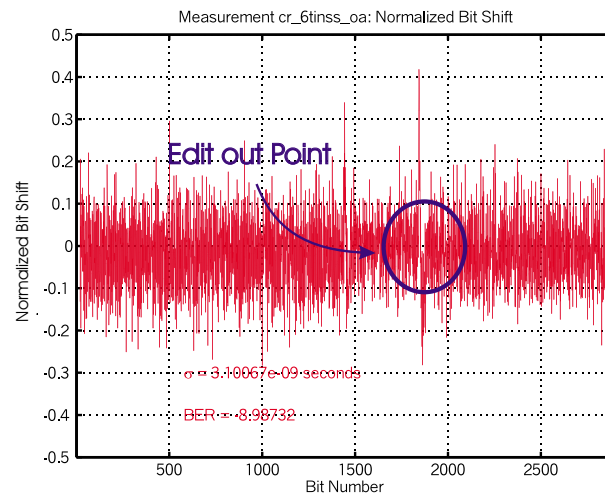
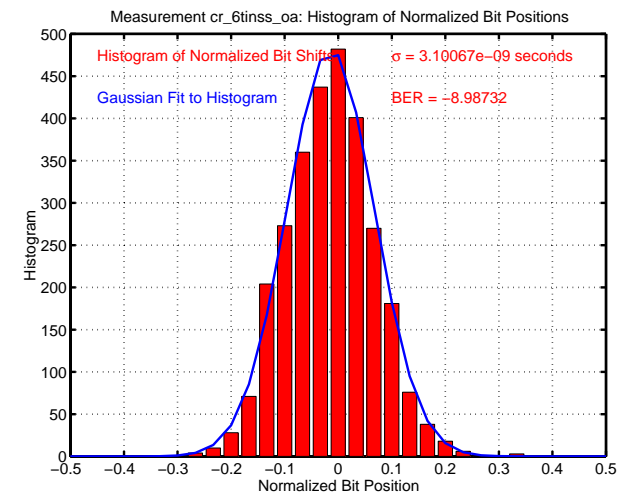
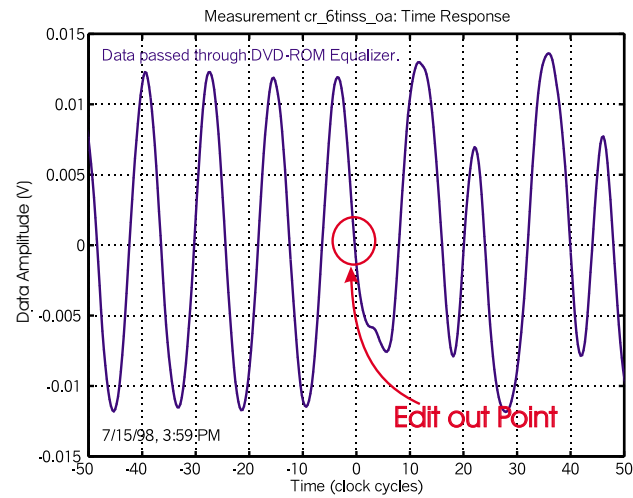
- Robust to offtrack, defocus, beam walk, & tilt



- A 6T pattern spliced into a 4T-8T pattern.
- Upper left: time response at the edit-in point
- Lower left: phase error for a data clock

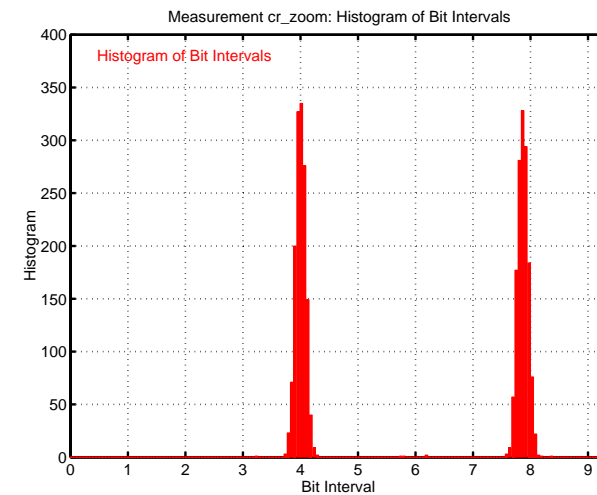
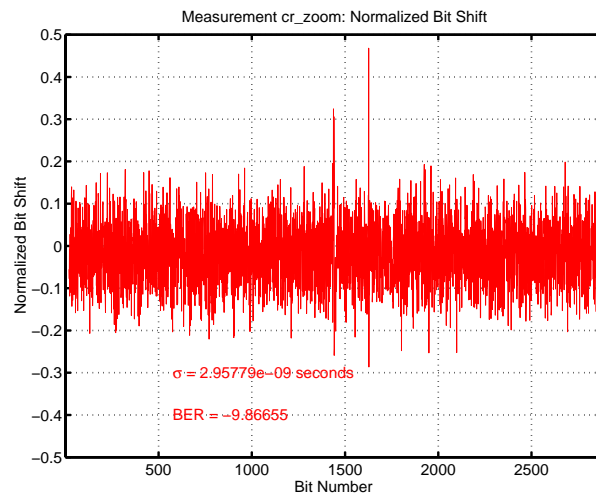
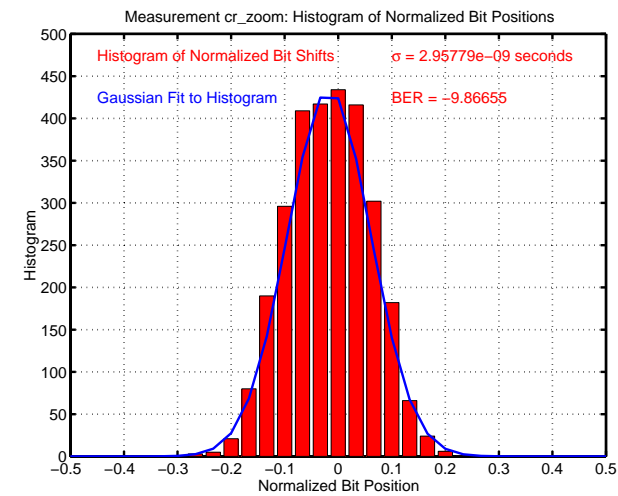
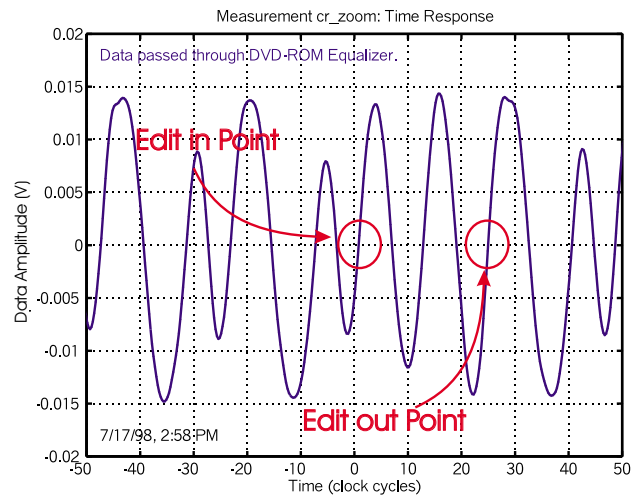
- Zoomed in on edit in point
- Upper right: histogram of normalized bit positions
- Lower right: histograms of the bit intervals.





- A 6T pattern spliced into a 4T-8T pattern.
- Upper left: time response at the edit-in point
- Lower left: phase error for a data clock

- Zoomed in on edit out point
- Upper right: histogram of normalized bit posn.
- Lower right: histograms of the bit intervals.

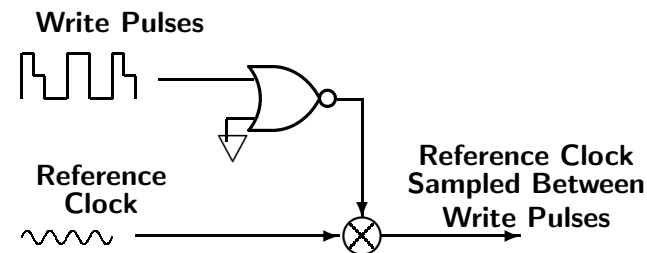
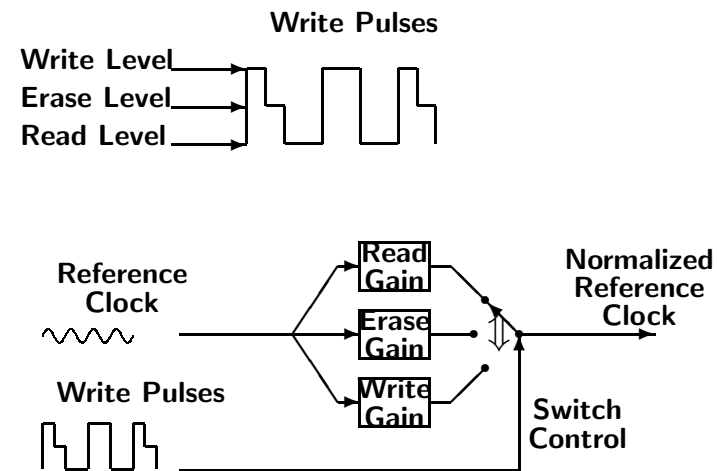


- A 2 bit 6T pattern spliced into a 4T-8T pattern.
- Upper left: time response at the edit-in point
- Lower left: phase error for a data clock

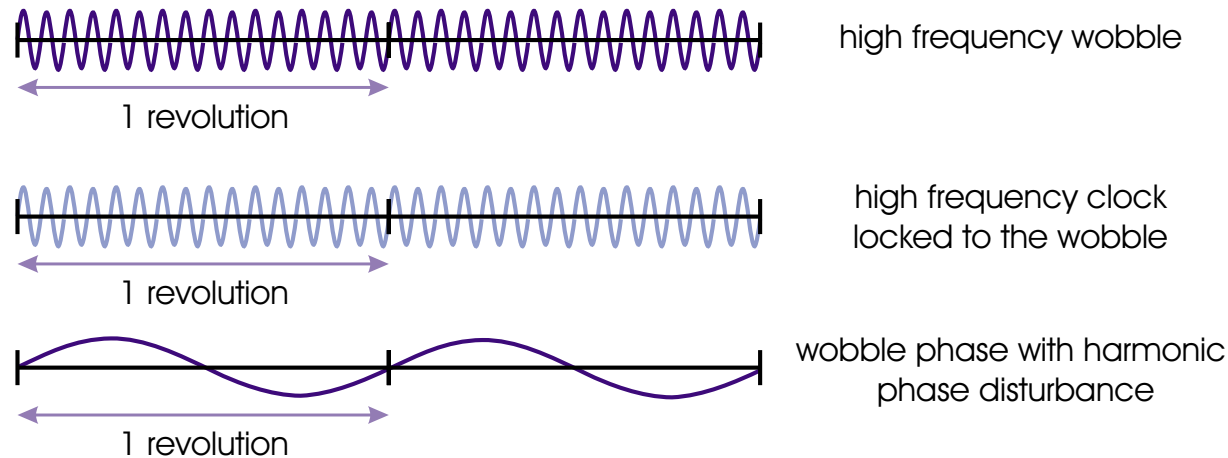
- Demonstrate this because we can.
- Upper right: histogram of normalized bit positions
- Lower right: histograms of the bit intervals.

## Laser Power Issues

- Laser power (and therefore signal power) has large changes between read, erase, & write levels (top drawing).
- Limiter/phase-detector based PLL is largely immune to amplitude shifts, but more susceptible to noise.
- Results from previous pages all done with limiter/phase-detector loops and 9T wobbles.
- If mixing PLL is used for noise immunity, power in the readback signal directly affects the gain of the PLL.
- Normalization circuits (used in servo loops) are too slow to respond.
- We know when the laser power will change
  - Gain schedule PLL to keep loop gain constant (middle drawing) or
  - sample reference clock between write & erase pulses (lower drawing).

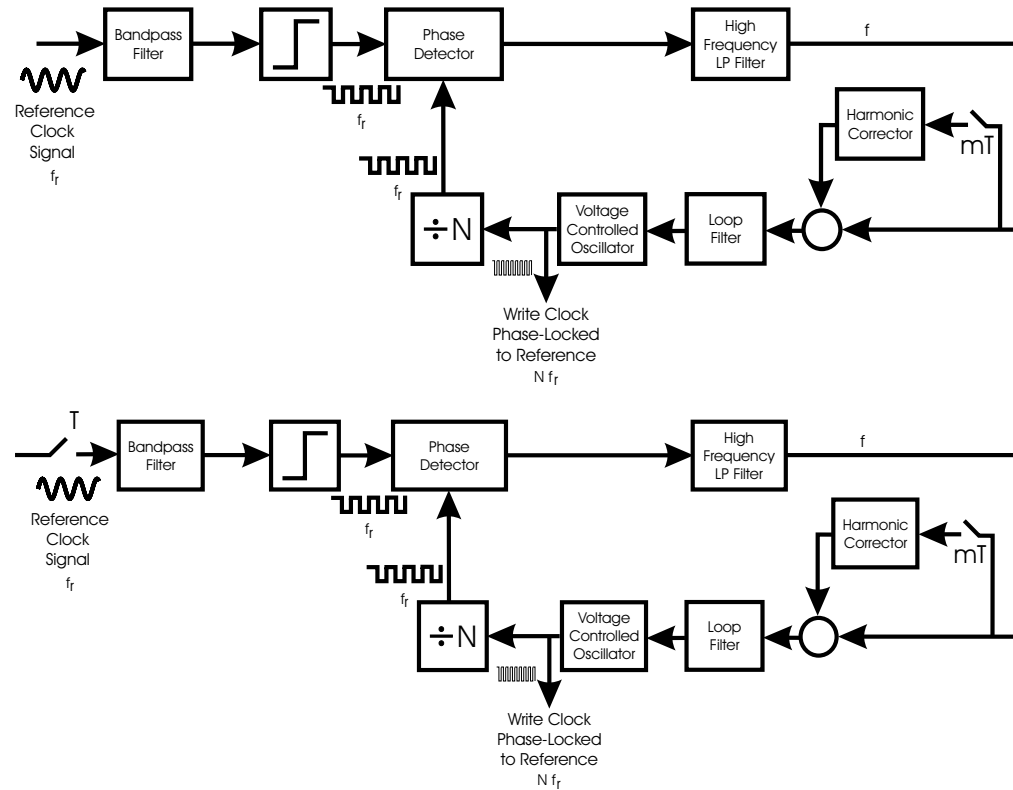


## Harmonic Cancellation of Harmonic Phase Errors in a PLL



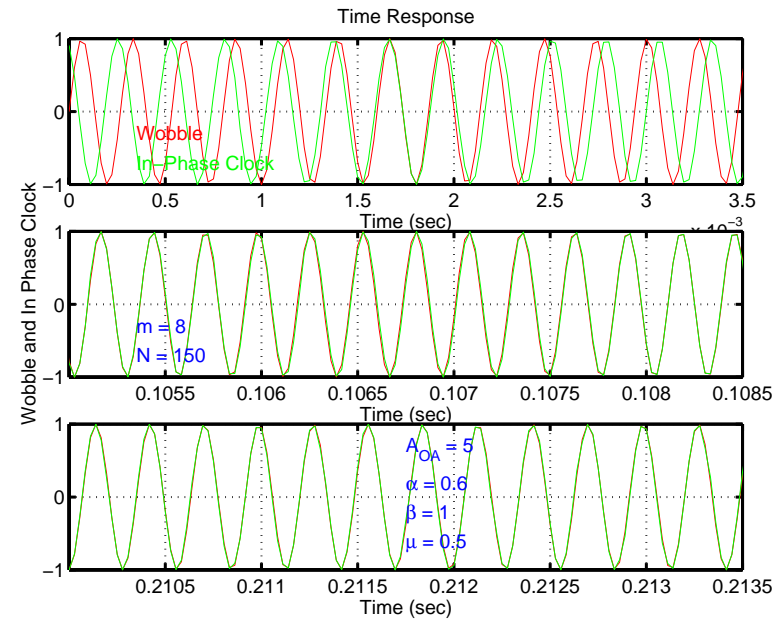
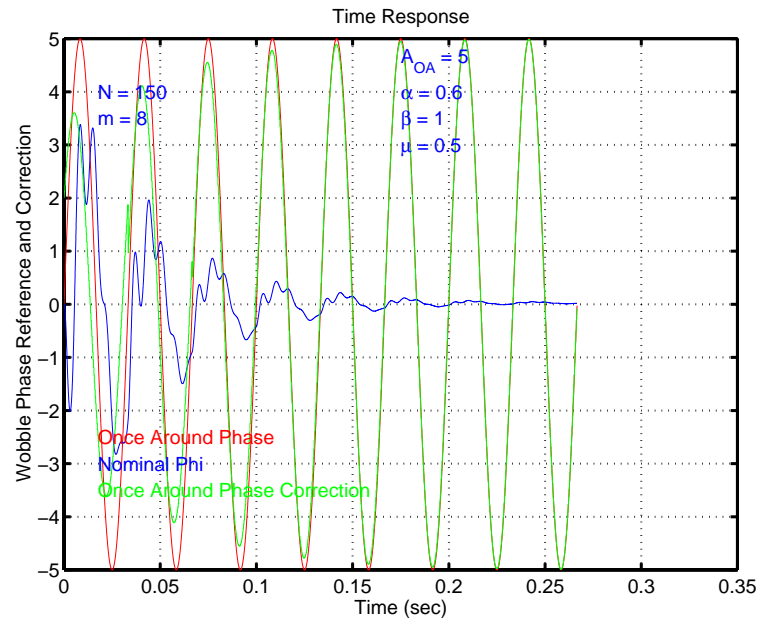
- Track eccentricity (mostly due to remounting of disk media on spindle) leads to harmonic errors in radial tracking loops and in timing loops.
- Harmonic correctors for tracking loops do not remove harmonic phase tracking errors in PLL.
- A desire to minimize the PLL bandwidth to reduce jitter leaves it unable to drive out all these errors. This problem became more severe when wobbles went from 9T to 31T (where T is a data clock period).
- Harmonic correction in the PLL can fix this. (Pay attention to where you are in the loop.)
- Note: This problem is very stiff. Clock in MHz with spindle at 30 Hz.
- Note: Harmonic cancellation or repetitive control can be used.

## Harmonic Locking & Sampled Harmonic Locking PLLs



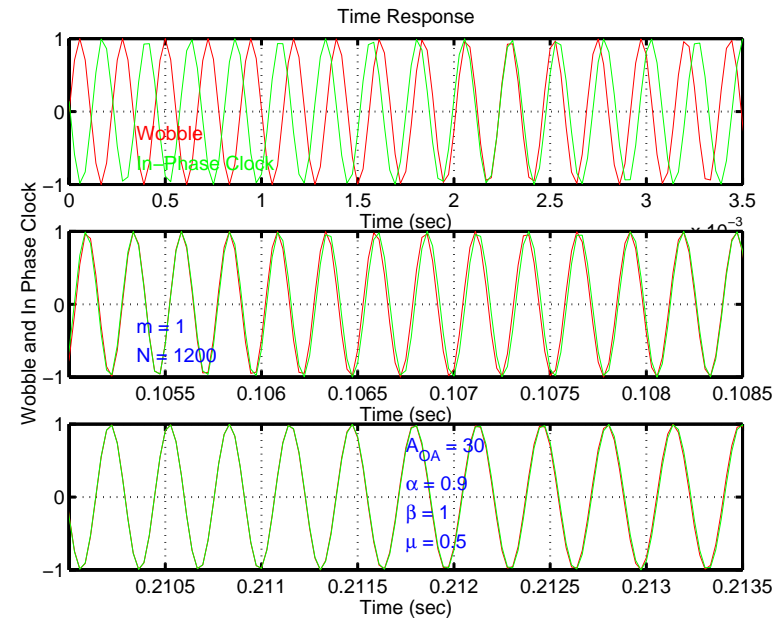
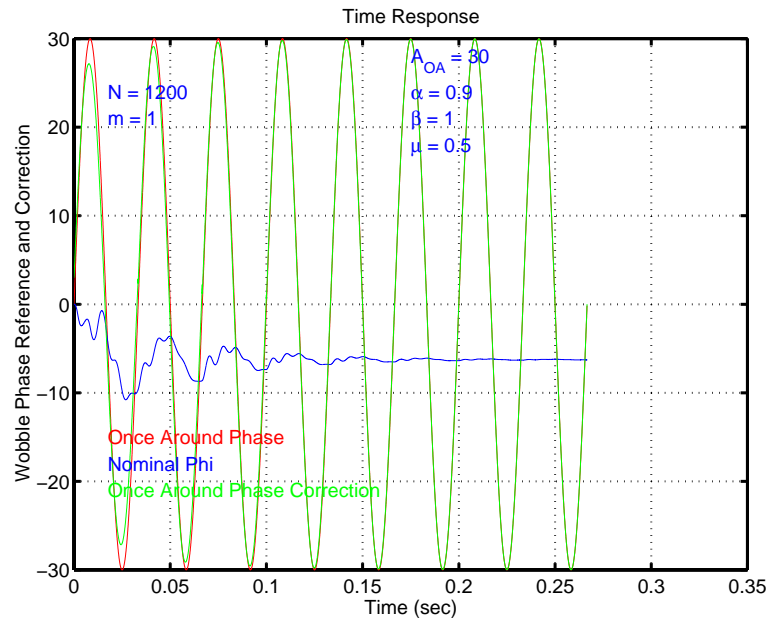
- Limiter/Phase-Detector handles amplitude variations
- Top loop has harmonic corrector tapping off of filtered phase error output,  $\Psi_f$ .
- Lower loop has multirate harmonic corrector tapping off of filtered phase error output,  $\Psi_f$ .
- Many configurations are possible for analysis/simulation.
- These configurations are implementable in hardware.

## Simulation Results for Multirate Harmonic Correcting PLL



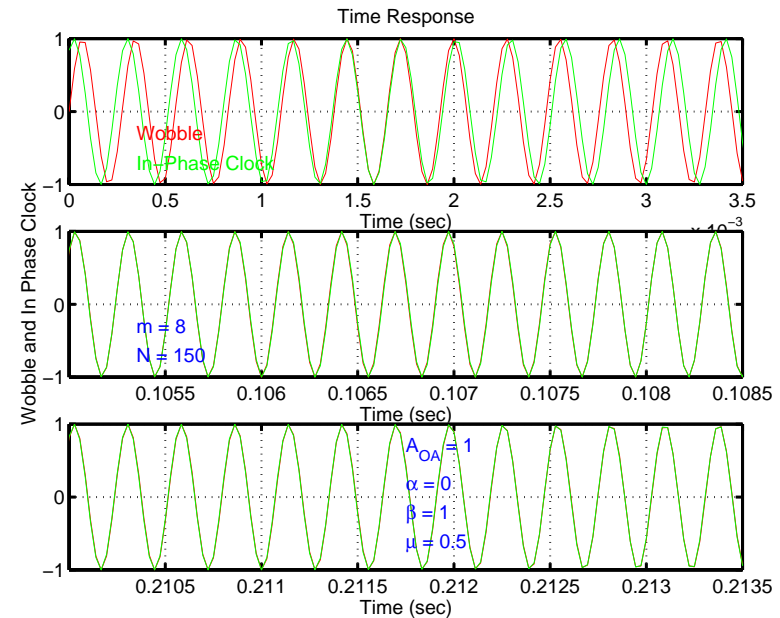
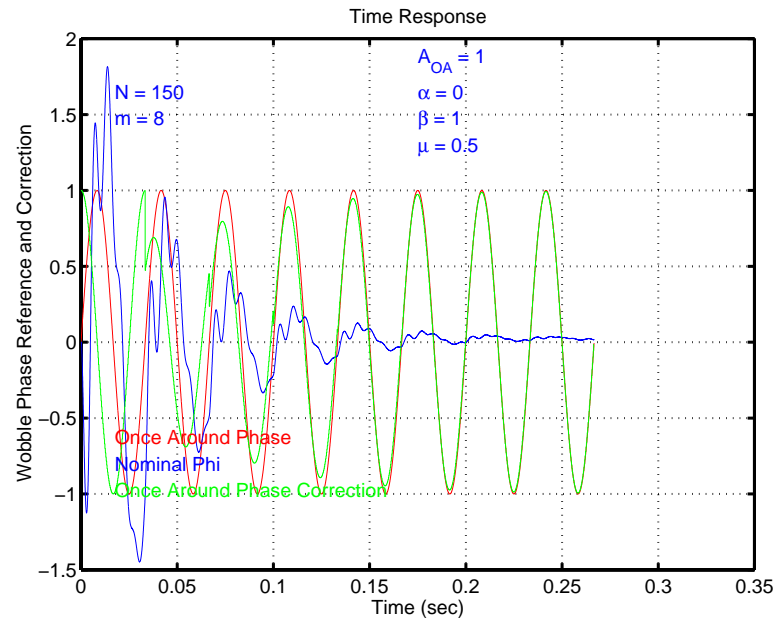
- Multi-rate once around correction with disturbance amplitude = 5 radians.
- Left plot shows phase; right plot shows clock.
- Harmonic corrector is subsampled at  $\frac{1}{8}$  times the sample rate of the PLL simulation.
- Specific parameters:  $N = 150 =$  wobble samples/revolution,  $m = 8 =$  subsample factor for harmonic corrector,  $\alpha = 0.6 =$  initial phase accuracy of corrector (1 = correct),  $\beta = 1 =$  initial amplitude accuracy of corrector (1 = correct),  $\mu = 0.5 =$  adaptation rate for adaptive feedforward compensation.

## Simulation Results for Single Rate Harmonic Correcting PLL



- Single-rate once around correction with disturbance amplitude = 30 radians.
- Left plot shows phase; right plot shows clock.
- Harmonic corrector is sampled at the sample rate of the PLL simulation.
- Specific parameters:  $N = 1200 =$  wobble samples/revolution,  $m = 1 =$  subsample factor for harmonic corrector,  $\alpha = 0.9 =$  initial phase accuracy of corrector (1 = correct),  $\beta = 1 =$  initial amplitude accuracy of corrector (1 = correct),  $\mu = 0.5 =$  adaptation rate for adaptive feedforward compensation.

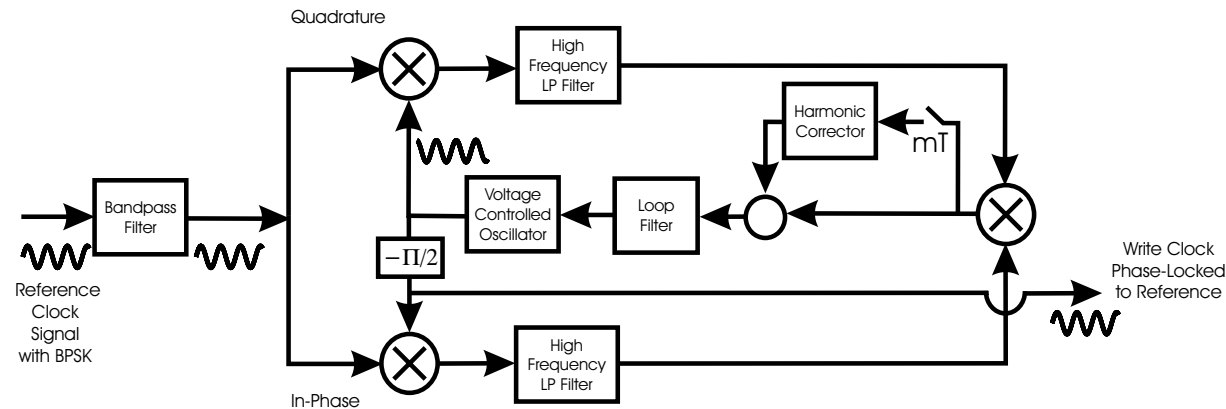
## Simulation Results for Multirate Harmonic Correcting PLL



- Multi-rate once around correction with disturbance amplitude = 1 radian.
- Left plot shows phase; right plot shows clock.
- Harmonic corrector is subsampled at  $\frac{1}{8}$  times the sample rate of the PLL simulation.
- Specific parameters:  $N = 150 =$  wobble samples/revolution,  $m = 8 =$  subsample factor for harmonic corrector,  $\alpha = 0.0 =$  initial phase accuracy of corrector (1 = correct),  $\beta = 1 =$  initial amplitude accuracy of corrector (1 = correct),  $\mu = 0.5 =$  adaptation rate for adaptive feedforward compensation.



## Harmonic Correcting Costas Loop



- A Mixing Costas Loop
- Loop has harmonic corrector tapping off of filtered phase error output,  $\Psi_f$ .
- This configurations are implementable in hardware.
- Provides improved performance for BPSK wobbles.

## Conclusions

- Bit accurate editing a reality.

This is closer to the DVD-ROM format than any other published results.

Only demonstration to get random rewritability in ROM compatible format.



- Write clock is very robust to:

Offtrack:	$\pm 30$ nm
Defocus:	$\pm 0.8$ $\mu$ m
Beam Walk:	$\pm 6\%$ of beam
Radial Tilt:	$\pm 0.3^\circ$
Tangential Tilt:	$\pm 0.6^\circ$

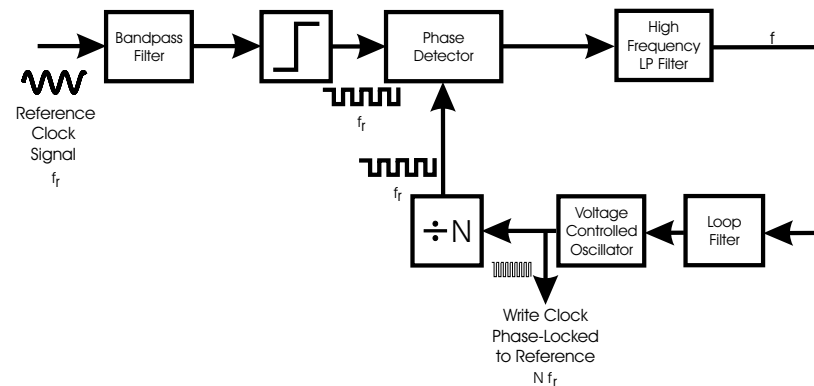
- Extra servo tricks can correct some drive related issues:
  - Limiter/phase-detector or gain scheduling for amplitude variations.
  - Harmonic cancellation for harmonic disturbances.
- Linkless editing forms a key property of the 4.7GB DVD+RW format.

## Backup Slides

- The following slides are not meant as part of the main presentation, but may be useful for answering questions.

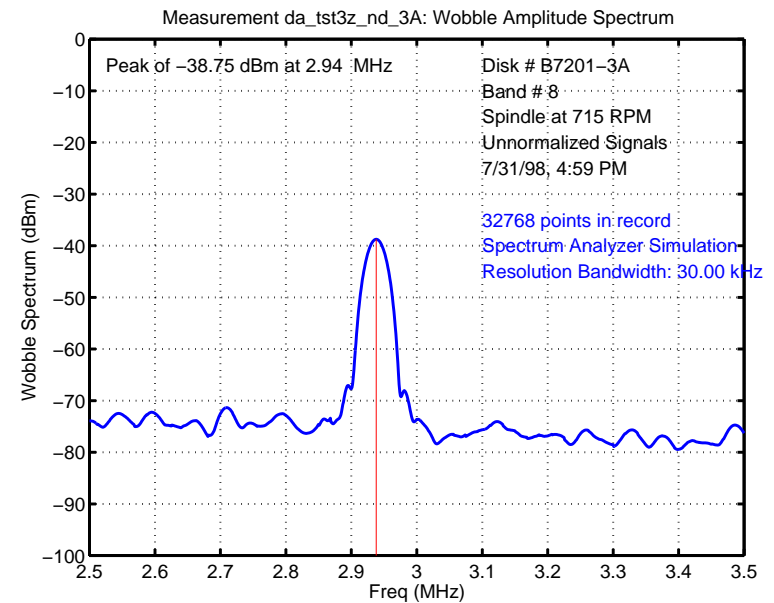
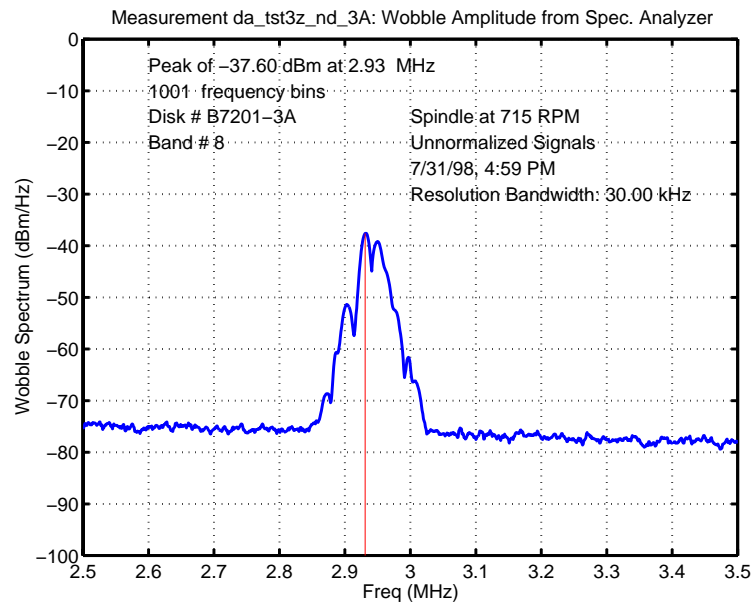
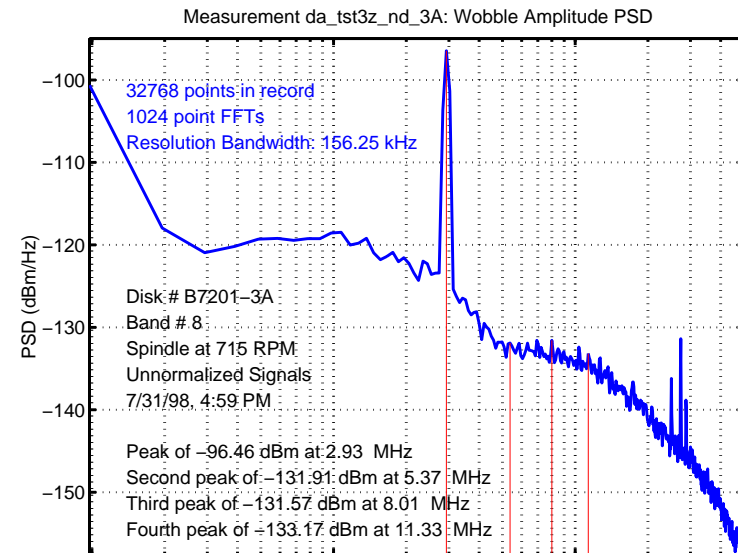
## Write Clock Generation Loop

- Generate write clock from reference signal
- Write clock is much higher frequency than reference structure
- Use harmonic locking loop
  - phase locks to reference signal
  - generates clock signal at  $N \times$  reference clock frequency
  - boosts jitter by  $N$ 
    - ⇒ want to minimize  $N$  for a given write frequency
    - ⇒ want to maximize reference clock frequency
- Various designs have been simulated.
- Limiter/Phase Detector hardware loop is used in linkless editing.
  - limiter insensitive to amplitude changes
  - other PLL architectures available as backup



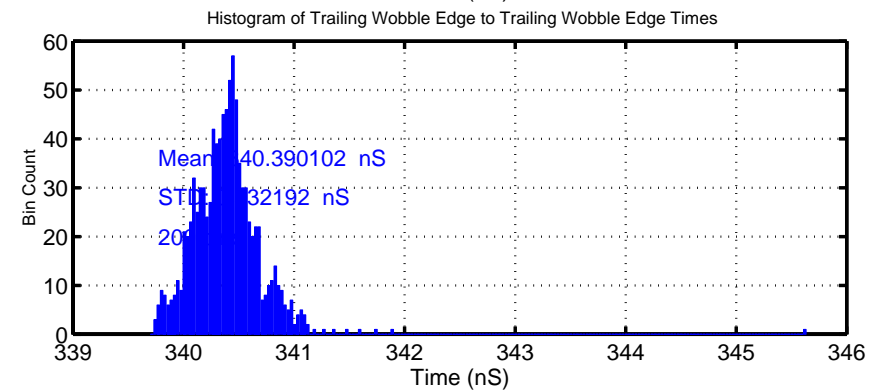
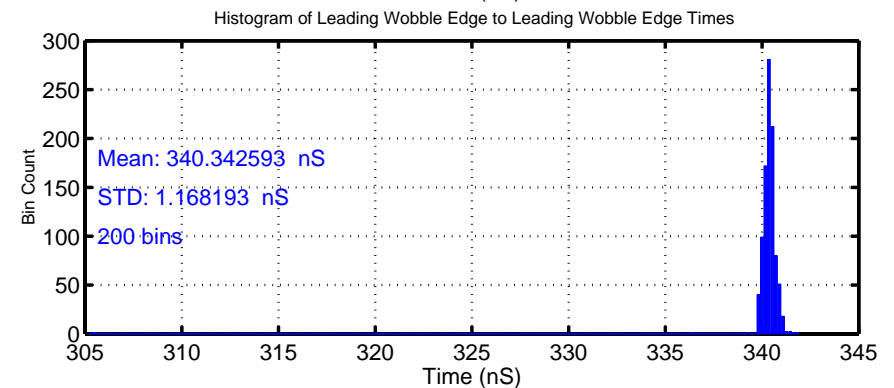
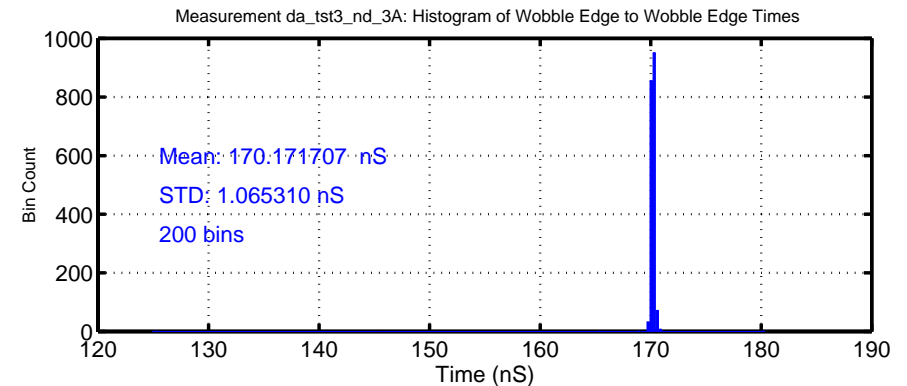
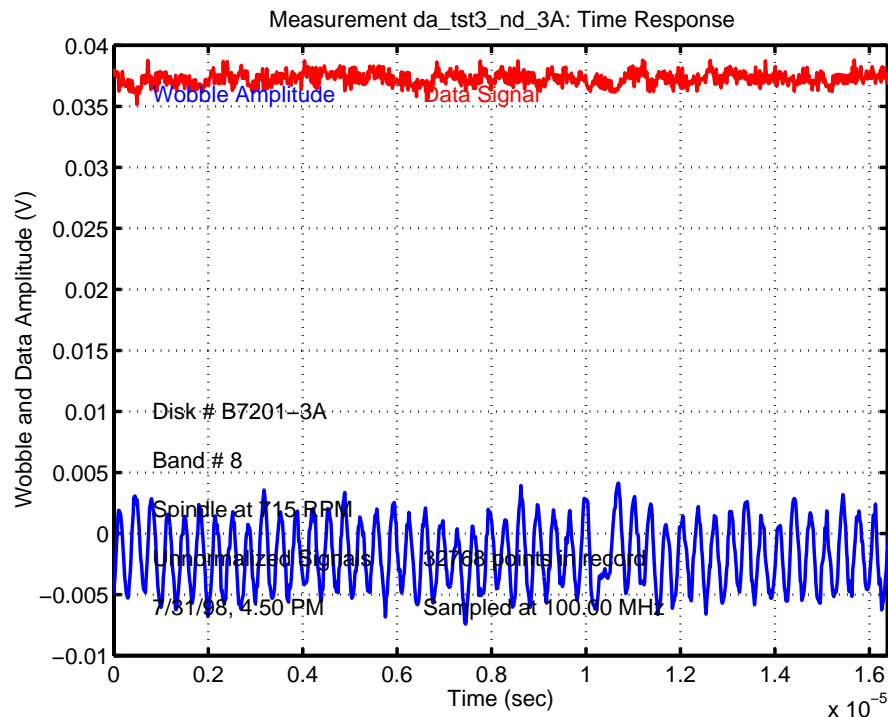
## Wobble Characterization: Frequency Domain

- To evaluate signal/noise levels
- Necessary to calibrate spectrum analyzer with scope based FFT methods
- Spectrum analyzer simulation has some greater capabilities than spectrum analyzer

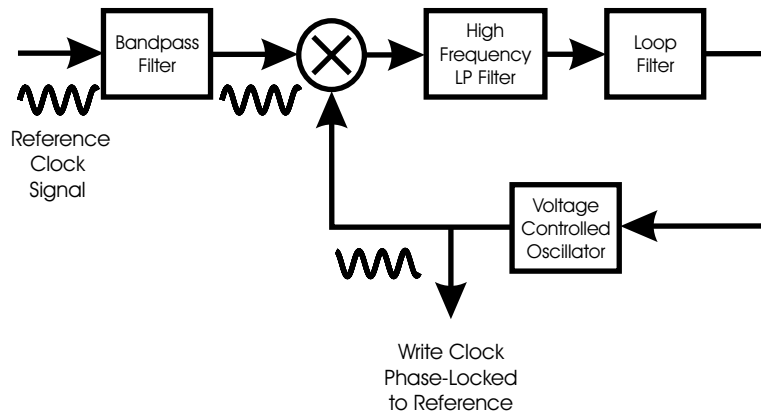


## Wobble Characterization: Time Domain

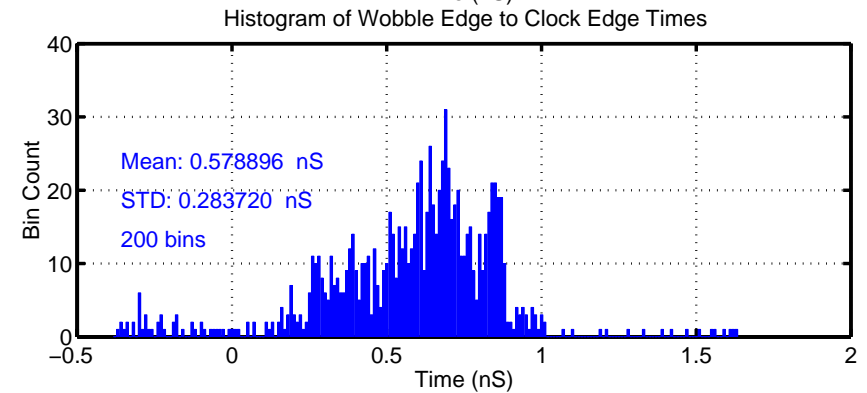
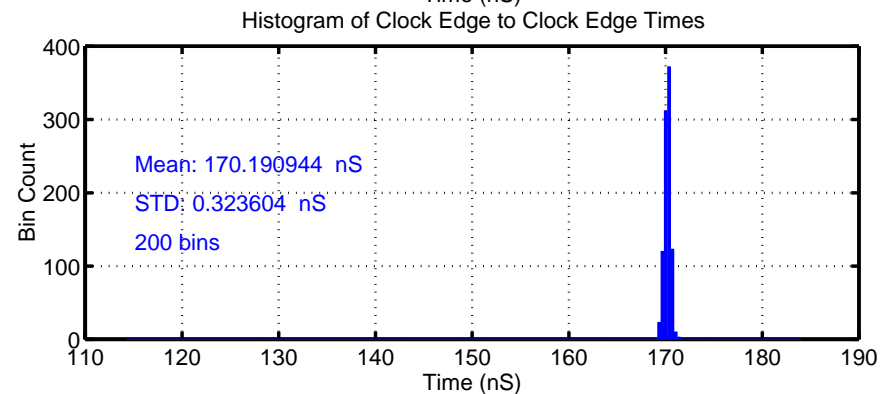
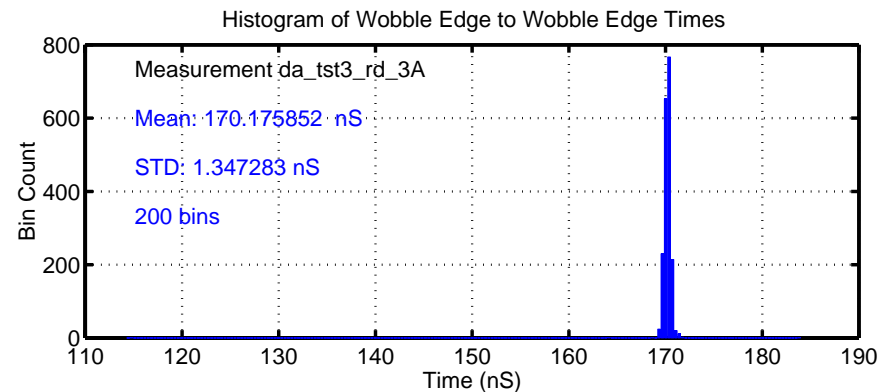
- To yield jitter analysis of wobble itself.
- Perform jitter calculation on filtered wobble signal.
- Edge to edge is most relevant for PLL.
- Leading edge to leading edge and trailing edge to trailing edge have significantly higher jitter.



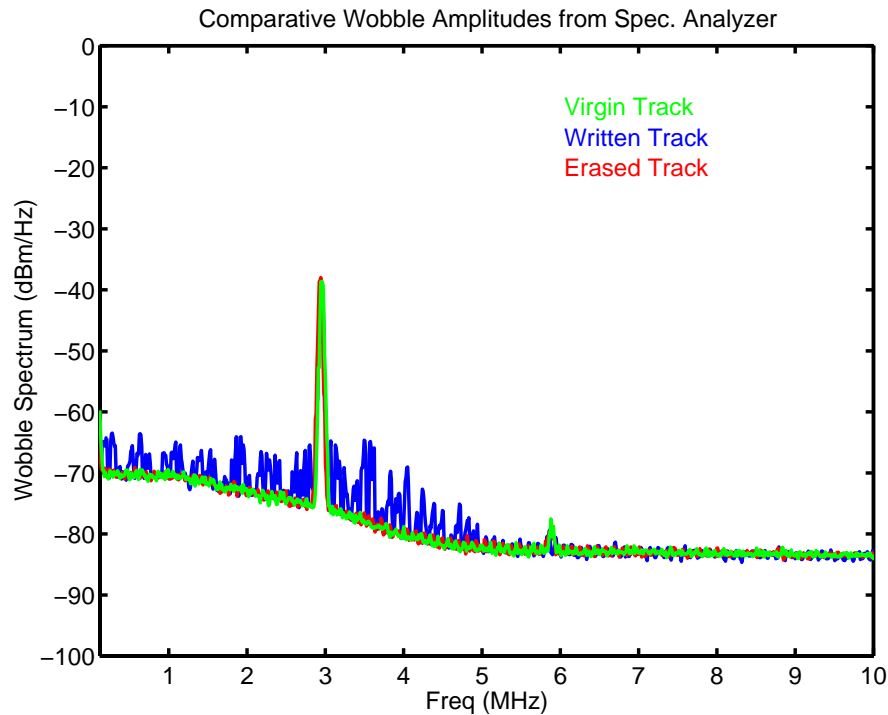
## Use PLL Simulation on Measured Wobble to Evaluate Quality of Clock



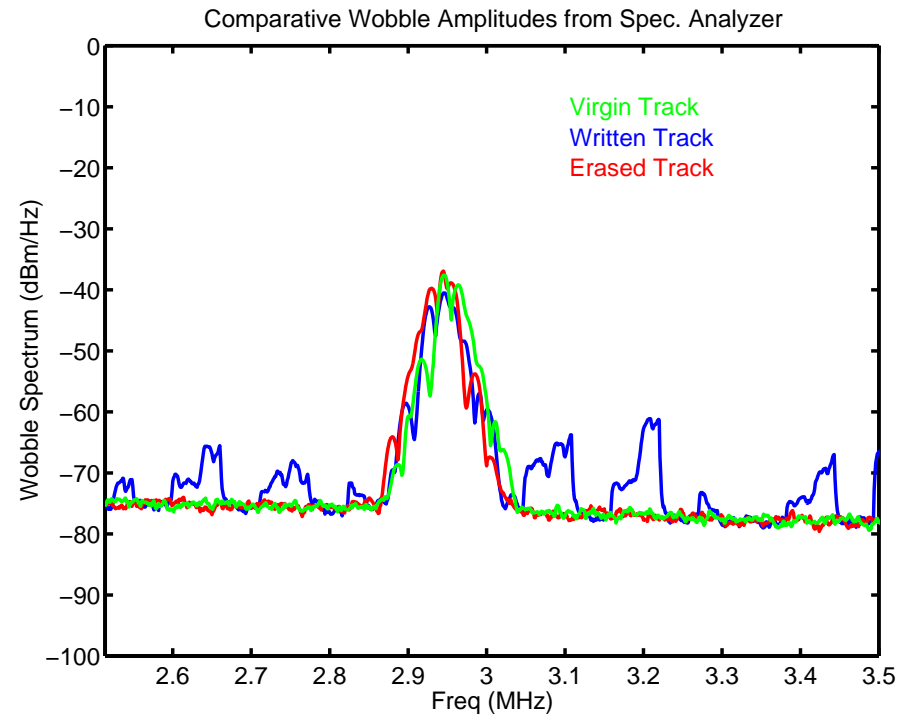
- Hardware loop used for writing.
- Simulation helps characterize achievable performance.
- Hardware loop uses XOR-type phase detector
  - ⇒ more timing sensitivity when simulated
  - ⇒ improved numerics using mixer
- Key measure for bit accurate edit is wobble edge to recovered clock edge jitter.
- Key measure for write quality is clock edge to clock edge jitter.
- Wobble to Clock Jitter < 1.0% of clock bit



## What Happens to Wobble When We Write and Erase?



Full frequency span.

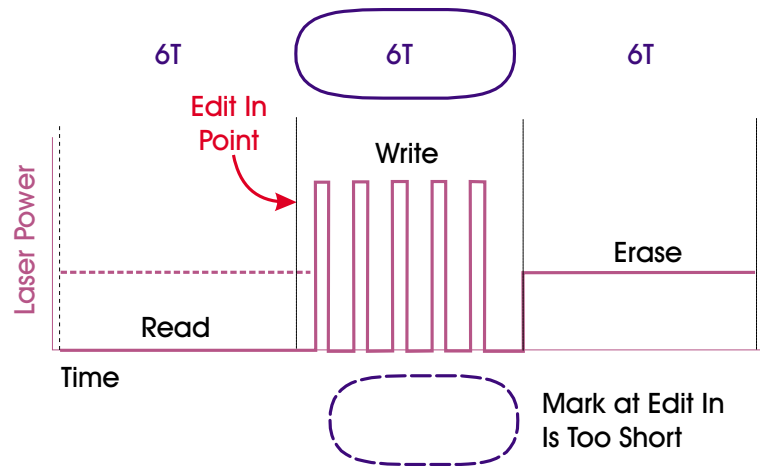


Zoomed in on wobble frequency.

- Not much.  $\Rightarrow$  No wobble erasure.
- Random data has significantly lower signal level at wobble frequency than wobble.
- Things improve as wobble amplitude goes up.
- Things improve as offsets are purged.



## Adjustments to Write Strategy in Edit In and Edit Out



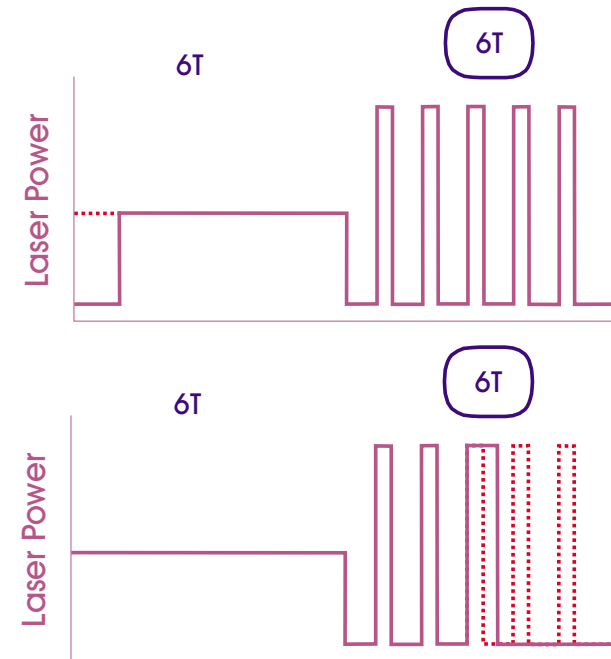
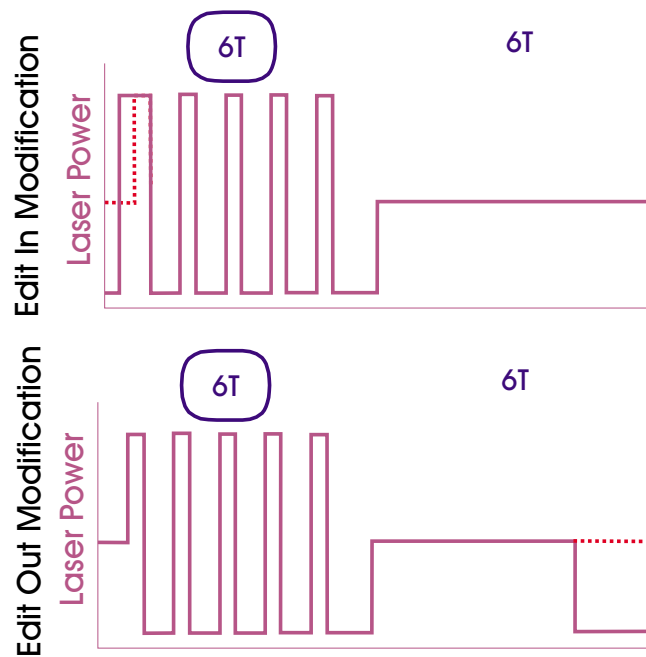
Problems at edit in:

- First mark too short, space too long

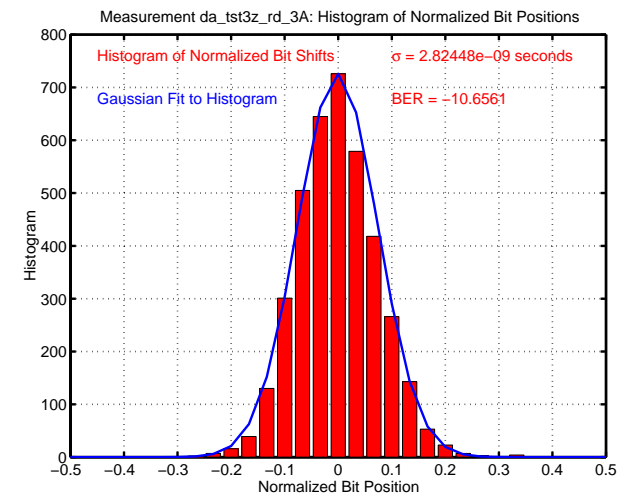
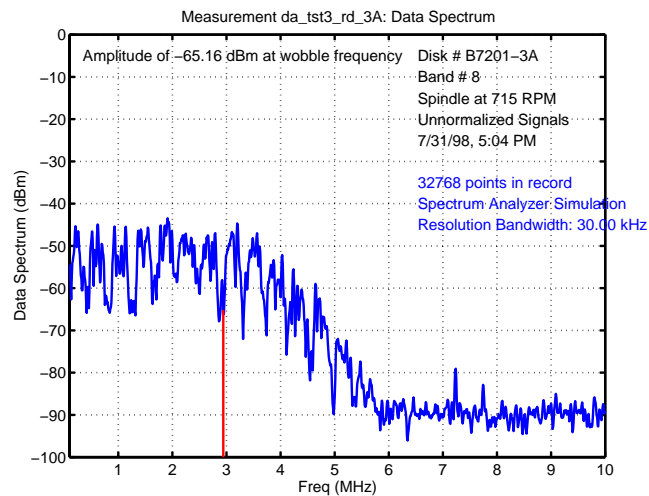
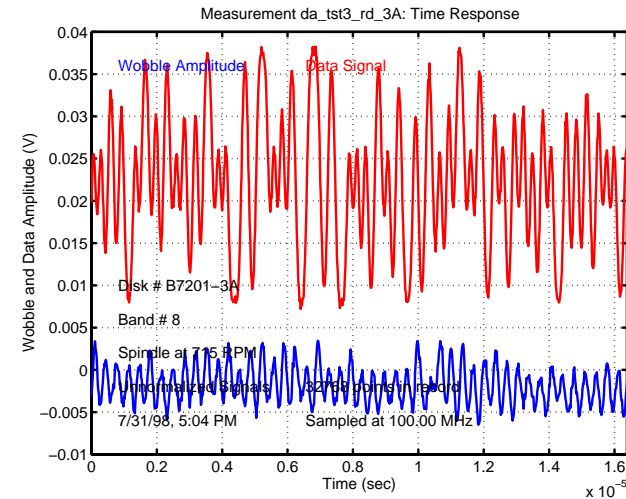
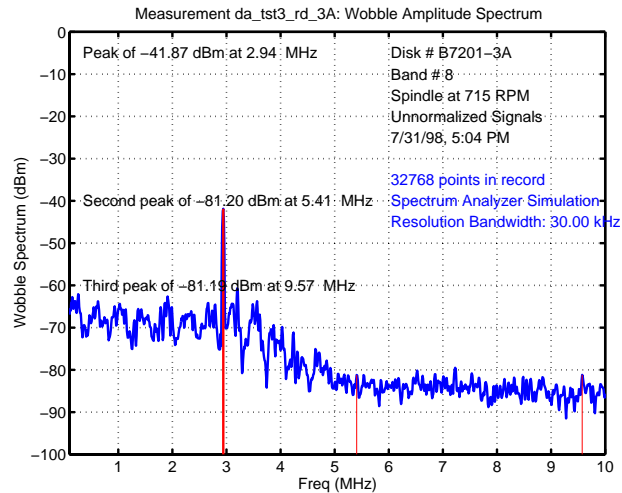
Problems at edit out:

- Mark and space too long

Adjust start & stop pulses to compensate



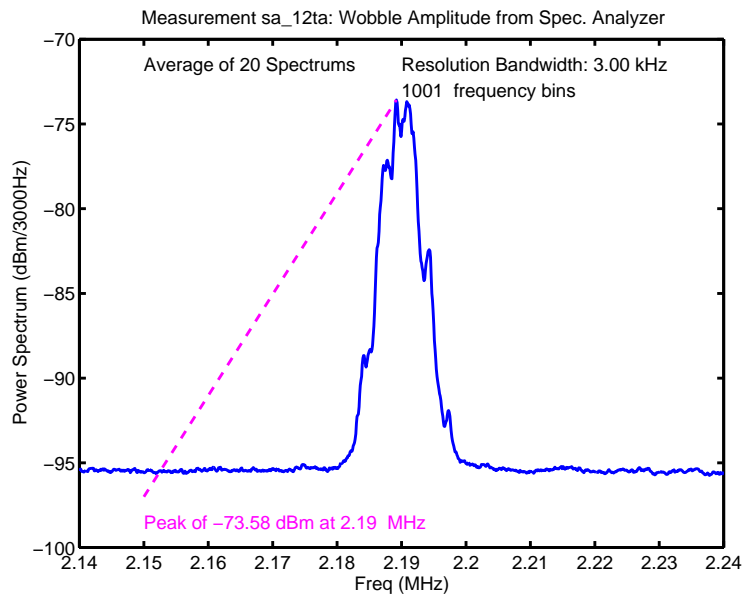
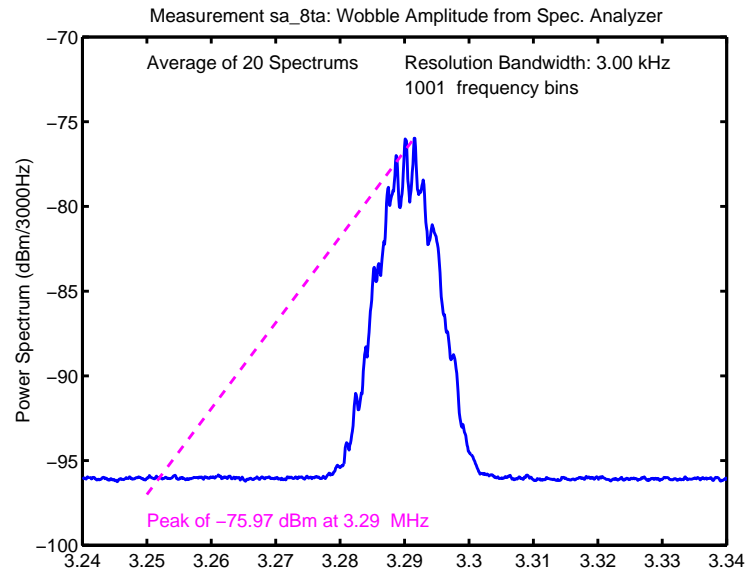
## Crosstalk Between Data and Wobbles is Small



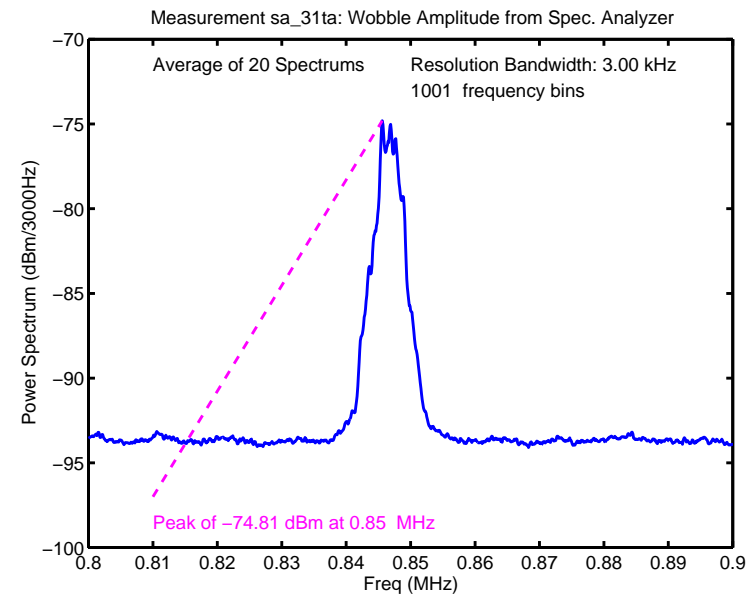
- Wobble into Data effect small vs. other “noises”
- no significant effect on bit error rate

- Data into Wobble related to offtrack
- mostly an issue with simple tones

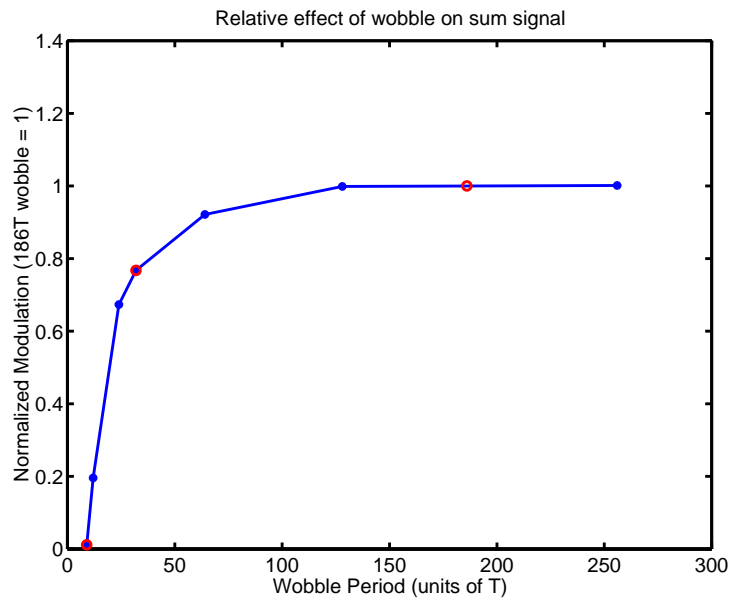
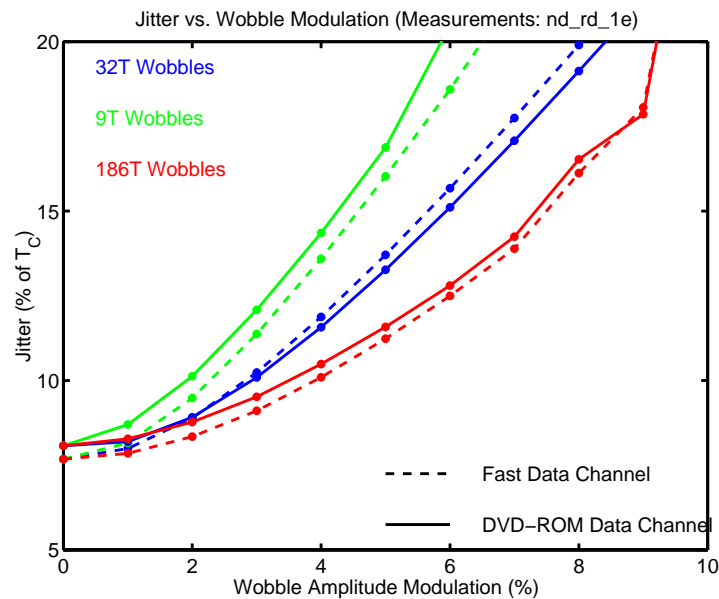
## Wobble Crosstalk into Data Channel



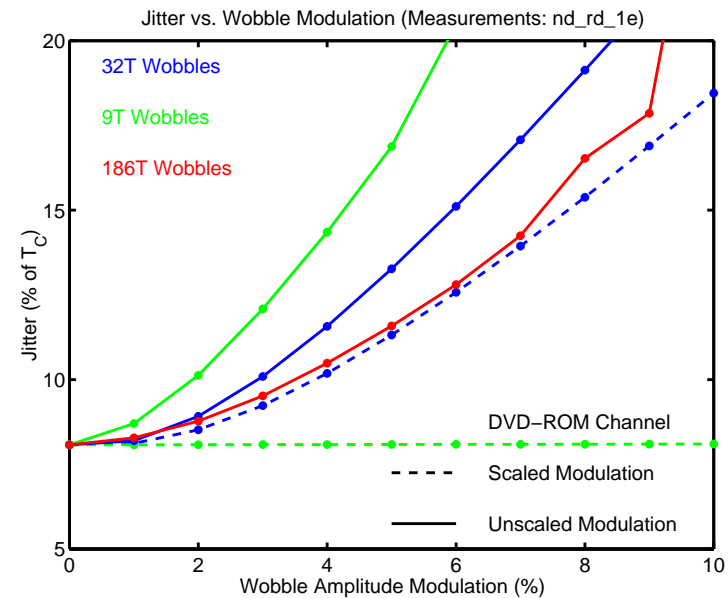
- Spectrum analyzer measurements of wobble modulation into data channel.
- No data on tracks.
- Plots are averages of 20 spectrums on the same track at different down-the-track locations.
- Differences between crosstalk peaks are relatively small.



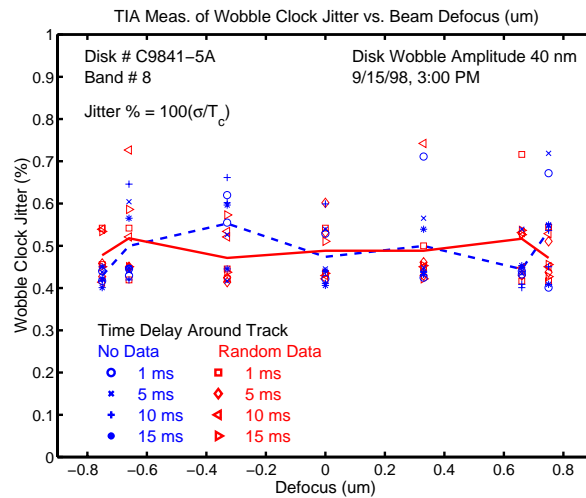
## Jitter Versus Wobble Crosstalk: A Simulation



- Data multiplied by  $1 + \alpha \sin(\omega_{wob}t)$ ,  
 $\alpha = 0, 0.01(1\%), \dots, 0.1(10\%)$
- “Fast Channel” provides slightly lower jitter than DVD-ROM PLL
- However, wobble does not enter into sum channel (A+B+C+D) in a uniform fashion
  - simulations based on diffraction orders
  - scale effective crosstalk of wobble into sum
  - normalized around 186 T (DVD-RW) wobbles having a scale of 1



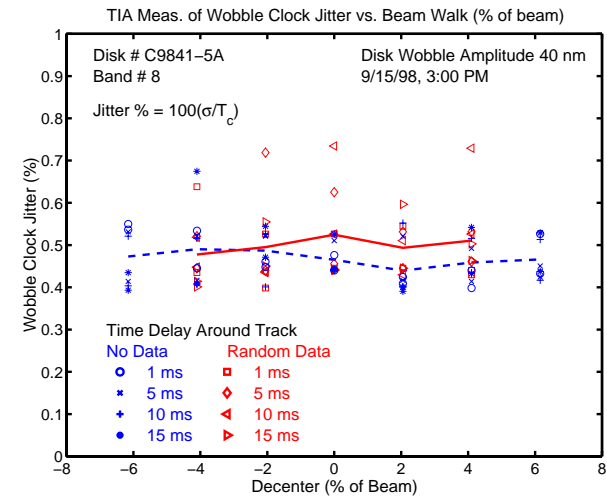
## Wobble Jitter vs. Defocus



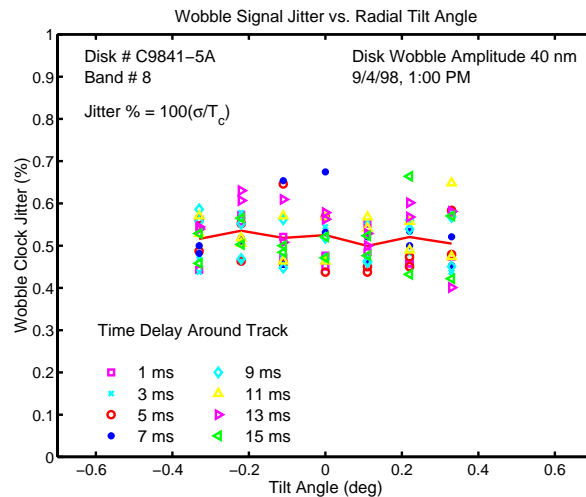
No Data

Random Data

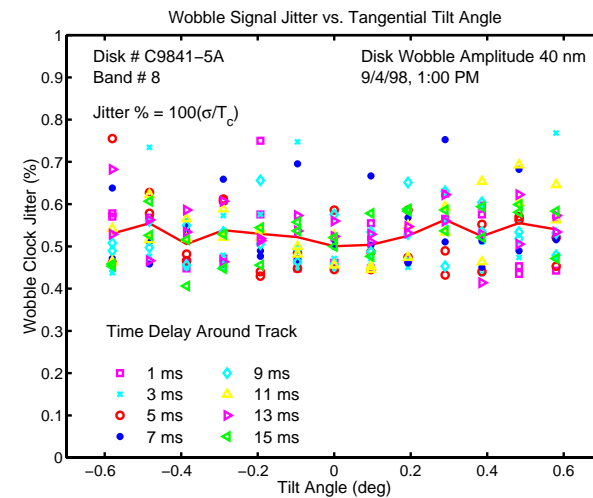
## Wobble Jitter vs. Beam Walk



## Wobble Jitter vs. Radial Tilt

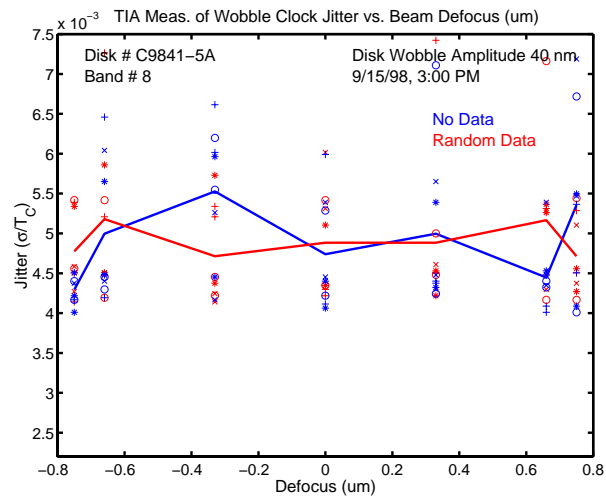
Random Data  
on Track  
& Adjacent  
Tracks

## Wobble Jitter vs. Tangential Tilt



- Wobble clock jitter from TIA: measure jitter on 2000 leading edges per revolution for 50 revolutions.

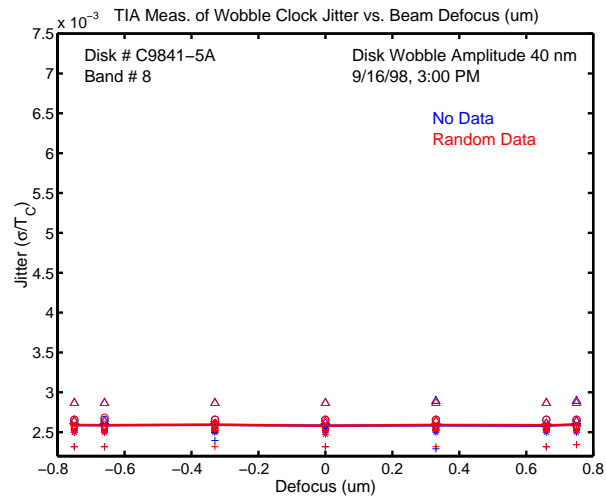
## Jitter vs. Defocus



Servo Lab

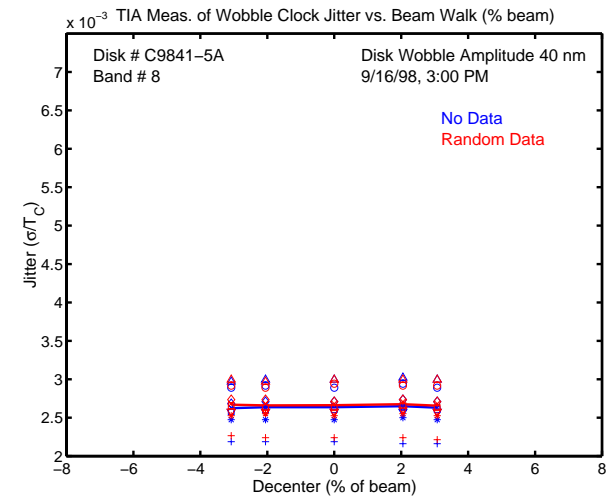
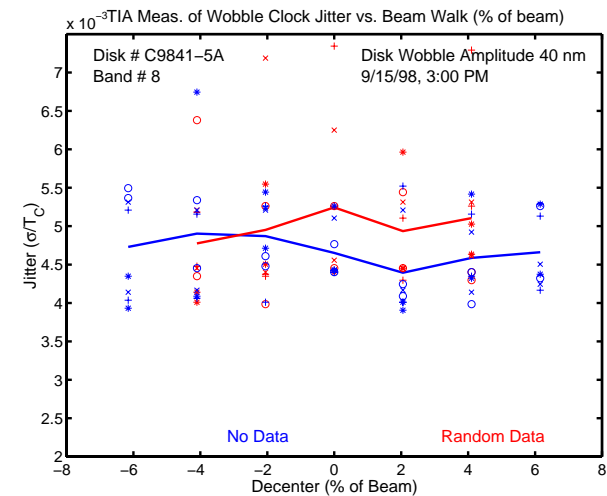
No Data

Random Data



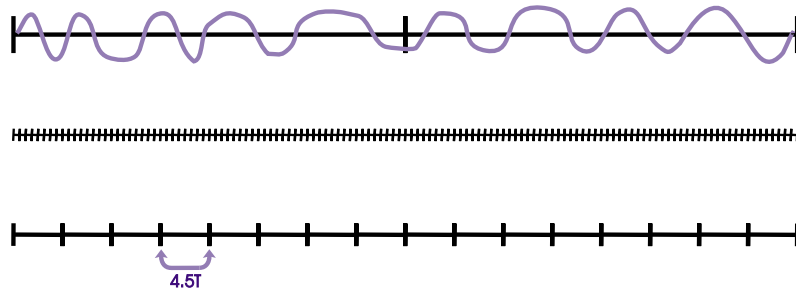
Media Lab

## Jitter vs. Beam Walk



- Wobble clock jitter from TIA: measure jitter on 2000 leading edges per revolution for 50 revolutions.
- Bad spindle has more effect than decenter (beam walk), defocus, offtrack, and position around track.

## Use Software Data Channel to Model DVD-ROM Data Channel

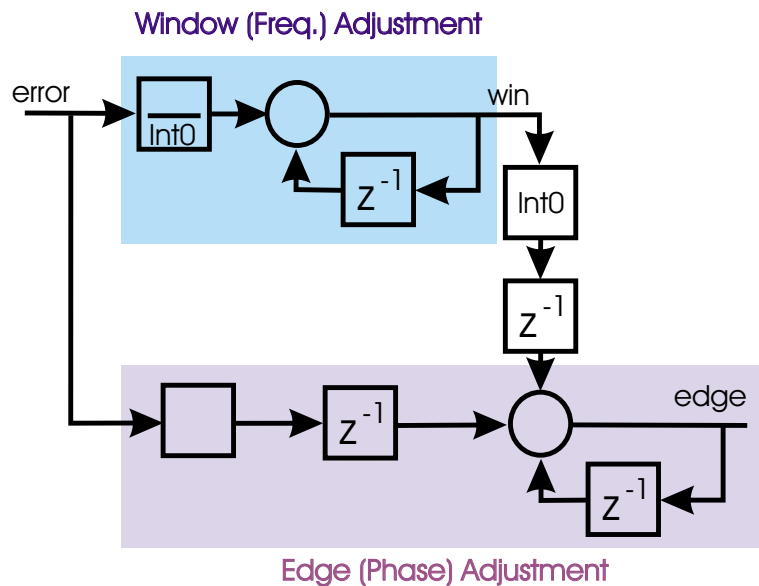


data signal

high sample rate  
on scopeeffective sample  
rate of PLL

- Scope samples data at 100 MHz
- Filtering done to match DVD-ROM at 100 MHz
- Average bit length  $\approx 4.5T_c$
- Use this as the effective sample rate for “zero-crossing” PLL

## Simplified PLL Analysis



## Difference Equations from Code

$$edge(k) = edge(k-1) + int0 * win(k-1) + \delta\phi(k-1)$$

$$\delta\phi(k) = \alpha * error(k)$$

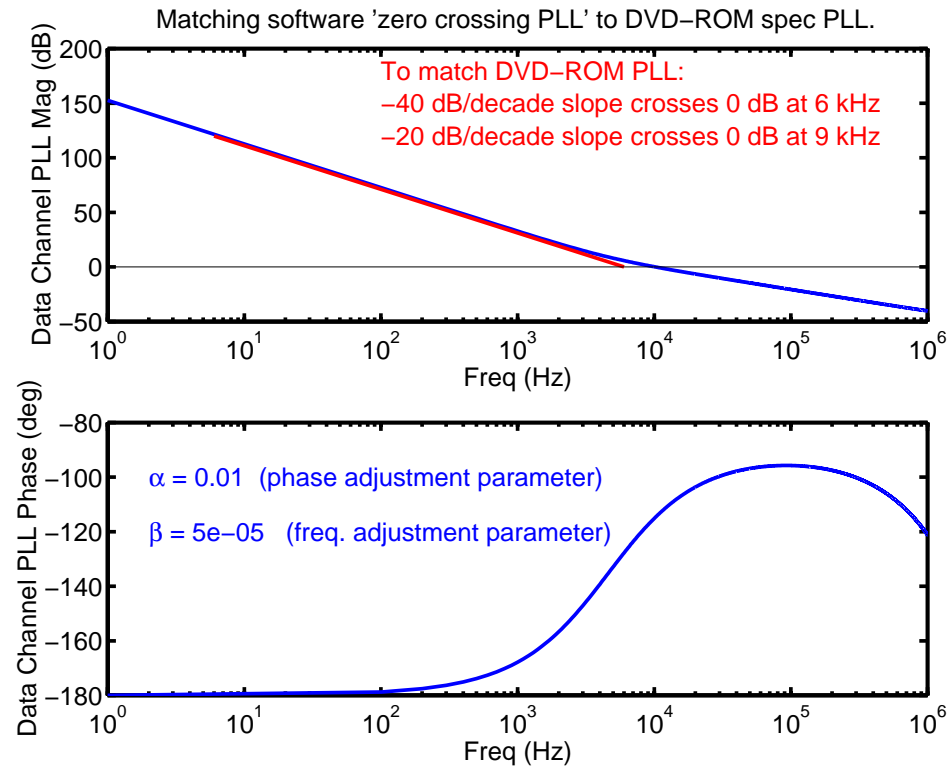
$$win(k) = win(k-1) + \beta * \frac{error(k)}{int0}$$

- Effective Sample Period  $\approx T_c * \text{average bit length} = 3.8160\text{e-8} * 4.5 \text{ S}$
- Effective sample rate  $\approx \frac{1}{1.7127\text{e-7}} = 5.8234 \text{ MHz}$
- Use the last filter, sampled at 5.8234 MHz, to match values of  $\alpha$  and  $\beta$  to DVD-ROM PLL.

### Translating to Z domain:

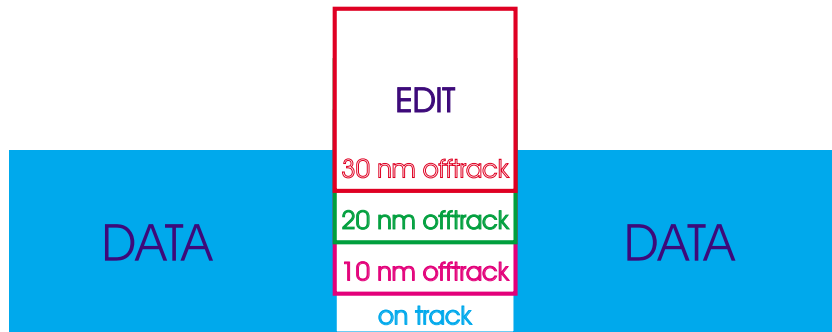
$$\begin{aligned} \text{win}(z)(1 - z^{-1}) &= \frac{\beta \text{error}(z)}{\text{int0}} \\ \frac{\text{win}(z)}{\text{error}(z)} &= \frac{\frac{\beta}{\text{int0}}}{1 - z^{-1}} \\ \text{edge}(z)(1 - z^{-1}) &= \text{int0}z^{-1}\text{win}(z) + \alpha z^{-1}\text{error} \end{aligned}$$

$$\frac{\text{edge}(z)}{\text{error}(z)} = \frac{z^{-1}}{(1 - z^{-1})^2} [\alpha + \beta - \alpha z^{-1}]$$

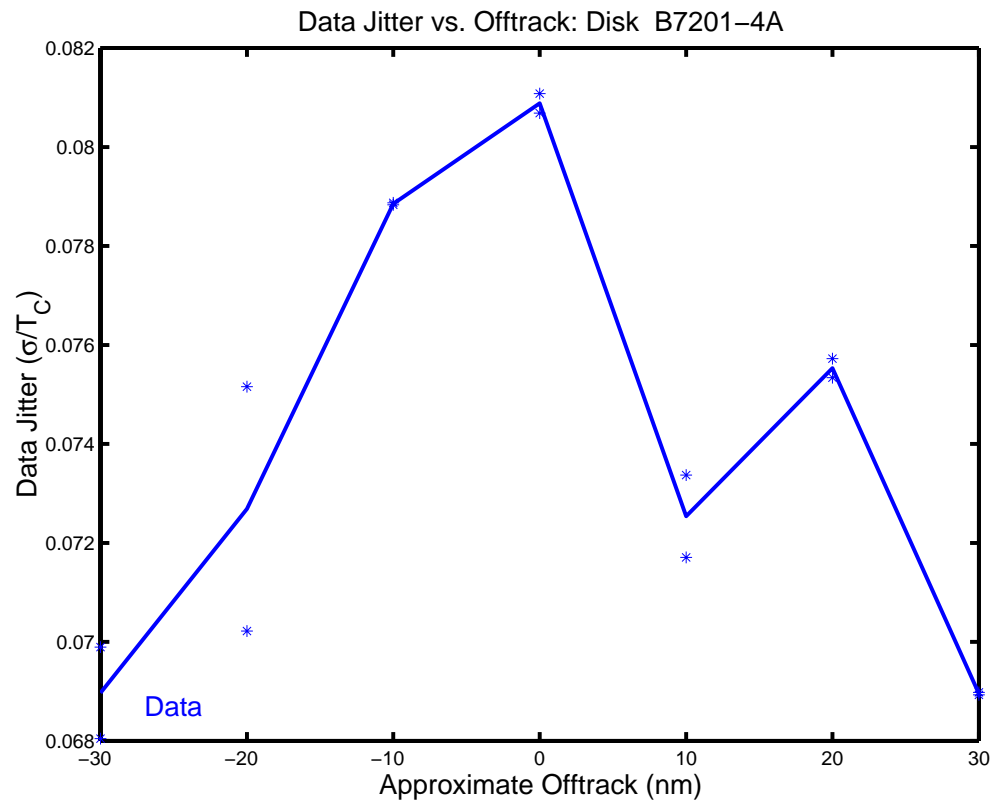




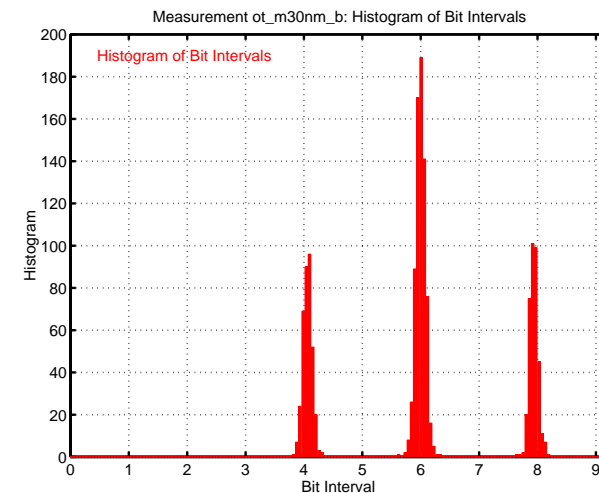
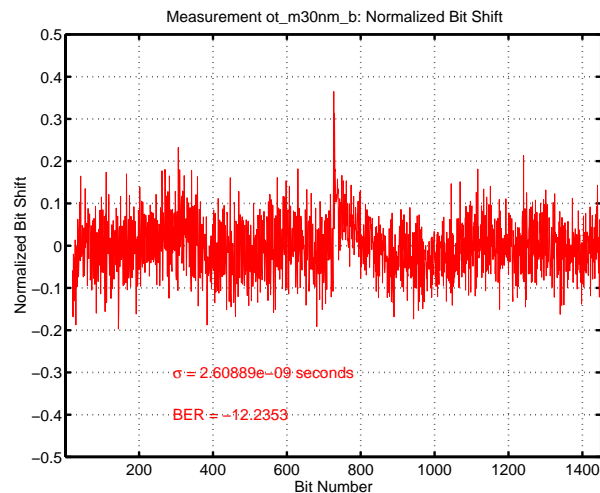
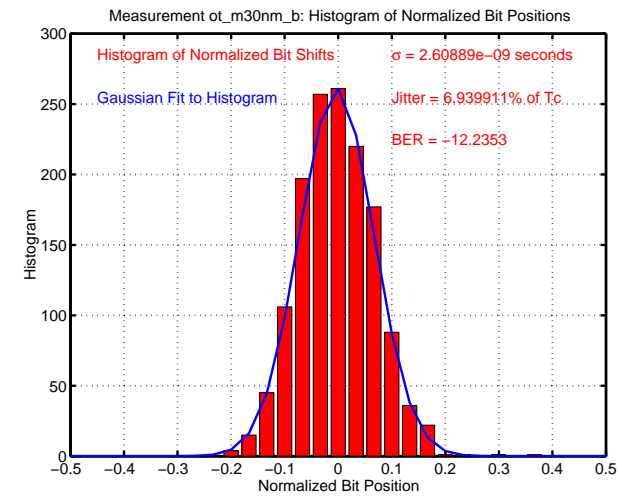
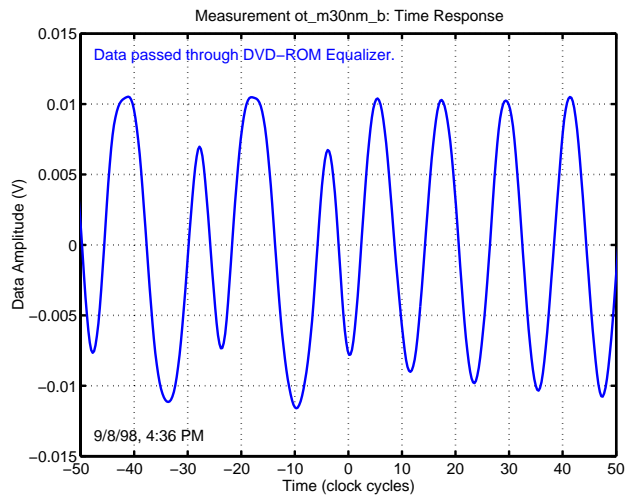
## Data Jitter Versus Offtrack Insert on 30 nm Wobble Disk



- Long write of 4T-8T pattern
- Edit insert with 6T pattern at various offtrack conditions.
- Data jitter calculated with lens on track



## Offtrack Measurement on 30 nm Wobble Disk



- This case is offtrack by -30 nm.
- Offtrack ranges in  $\pm 30$  nm produce no bit errors.